

FIG. 1

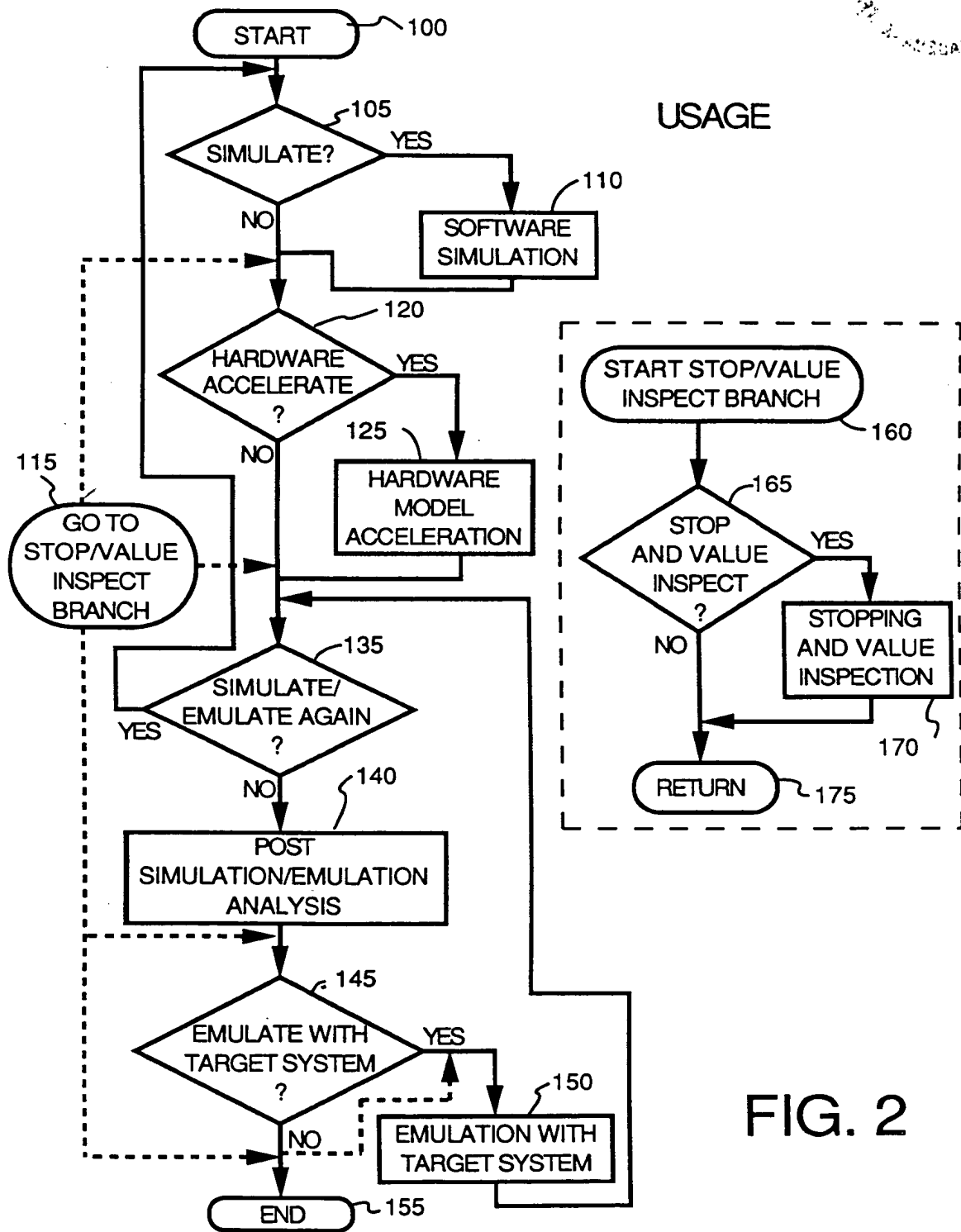
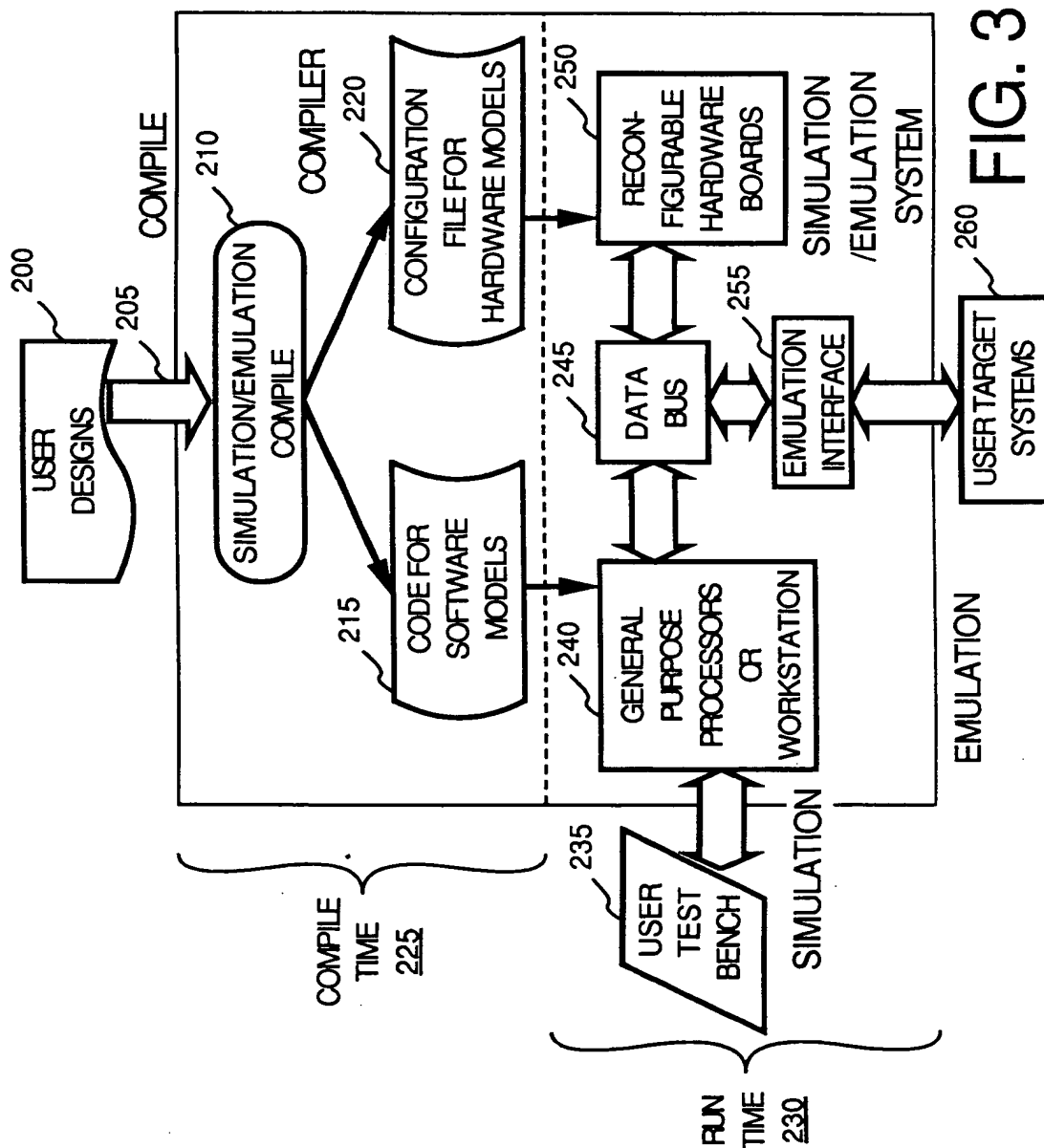


FIG. 2



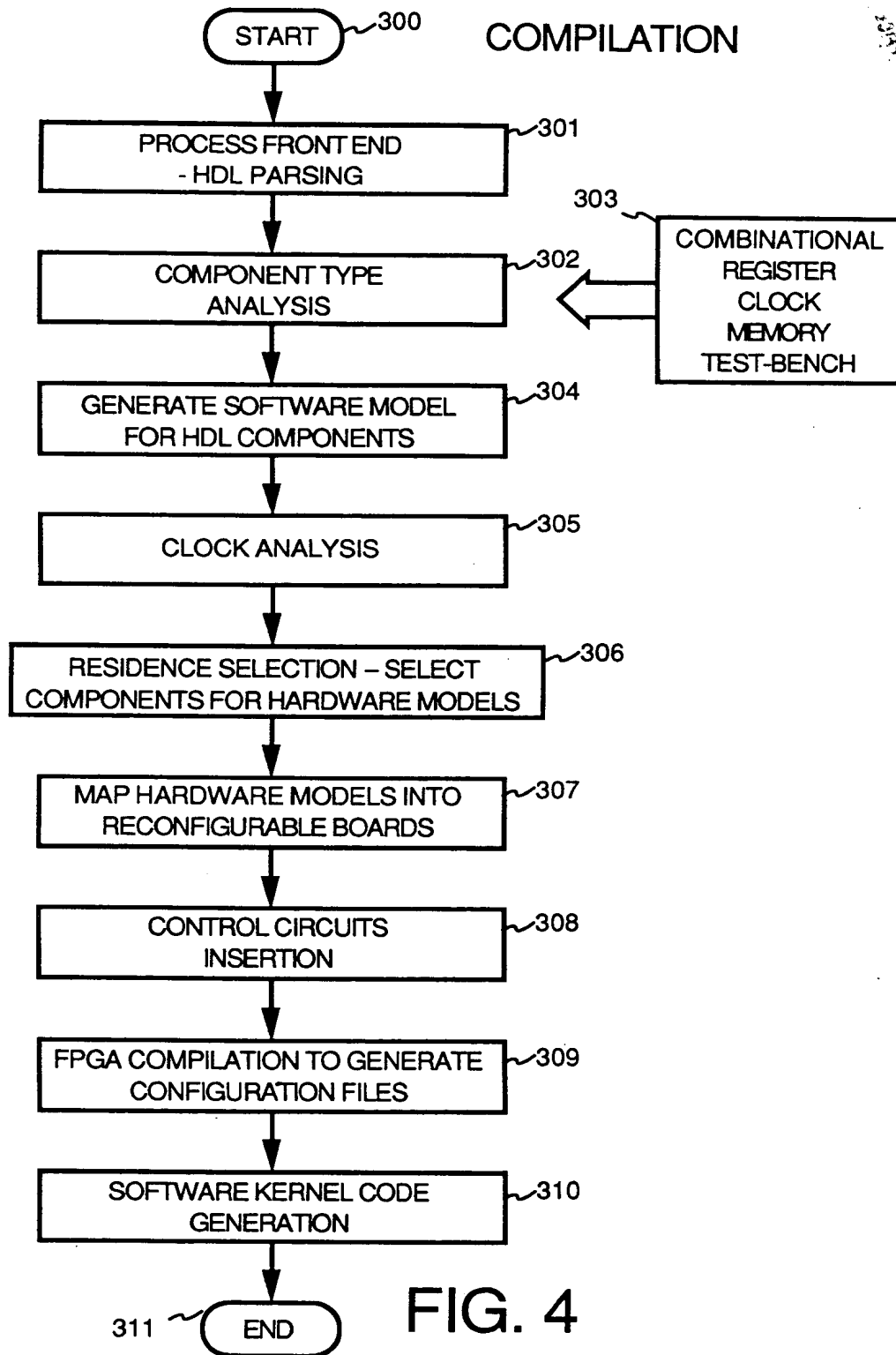


FIG. 4

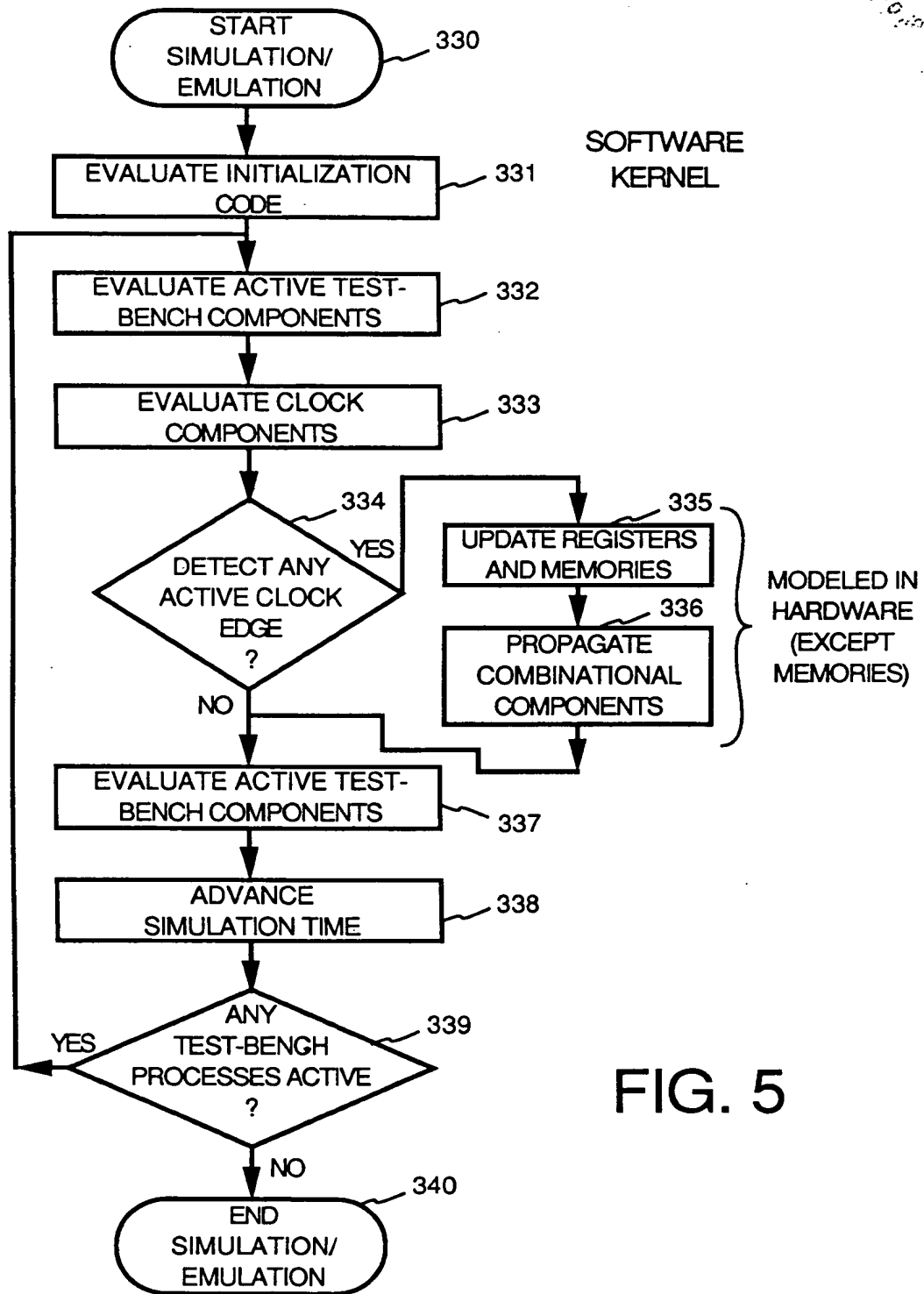


FIG. 5

MAPPING HARDWARE MODELS TO RECONFIGURABLE BOARDS

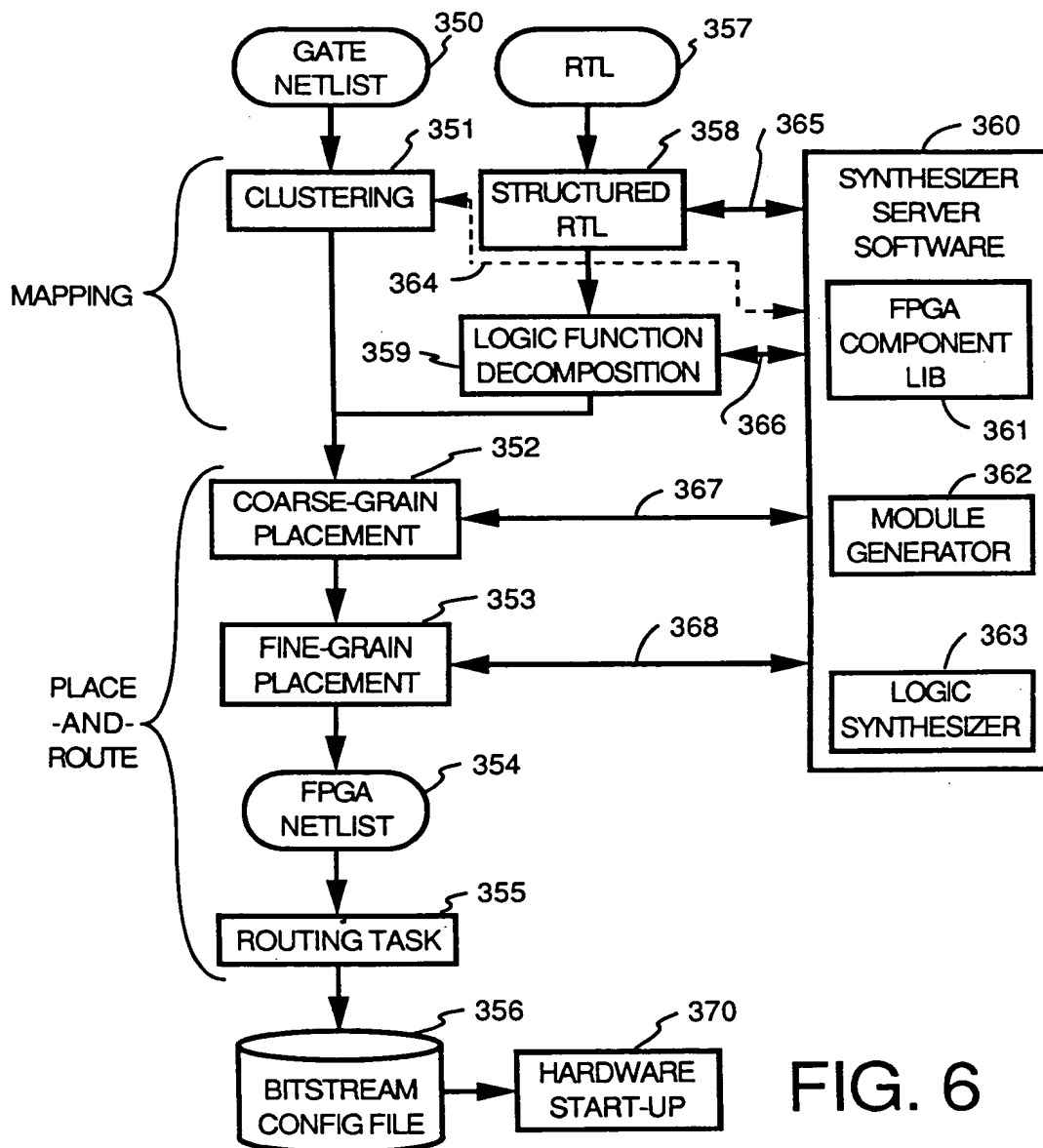


FIG. 6

	F11	F12	F13	F14	F21	F22	F23	F24	F31	F32	F33	F34	F41	F42	F43	F44
F11	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
F12	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
F13	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0
F14	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1
F21	1	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0
F22	0	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0
F23	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	0
F24	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
F31	1	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
F32	0	1	0	0	0	1	0	0	1	1	1	1	0	1	0	0
F33	0	0	1	0	0	0	1	0	1	1	1	1	0	0	1	0
F34	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0	1
F41	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1
F42	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1
F43	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1
F44	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1

FIG. 7



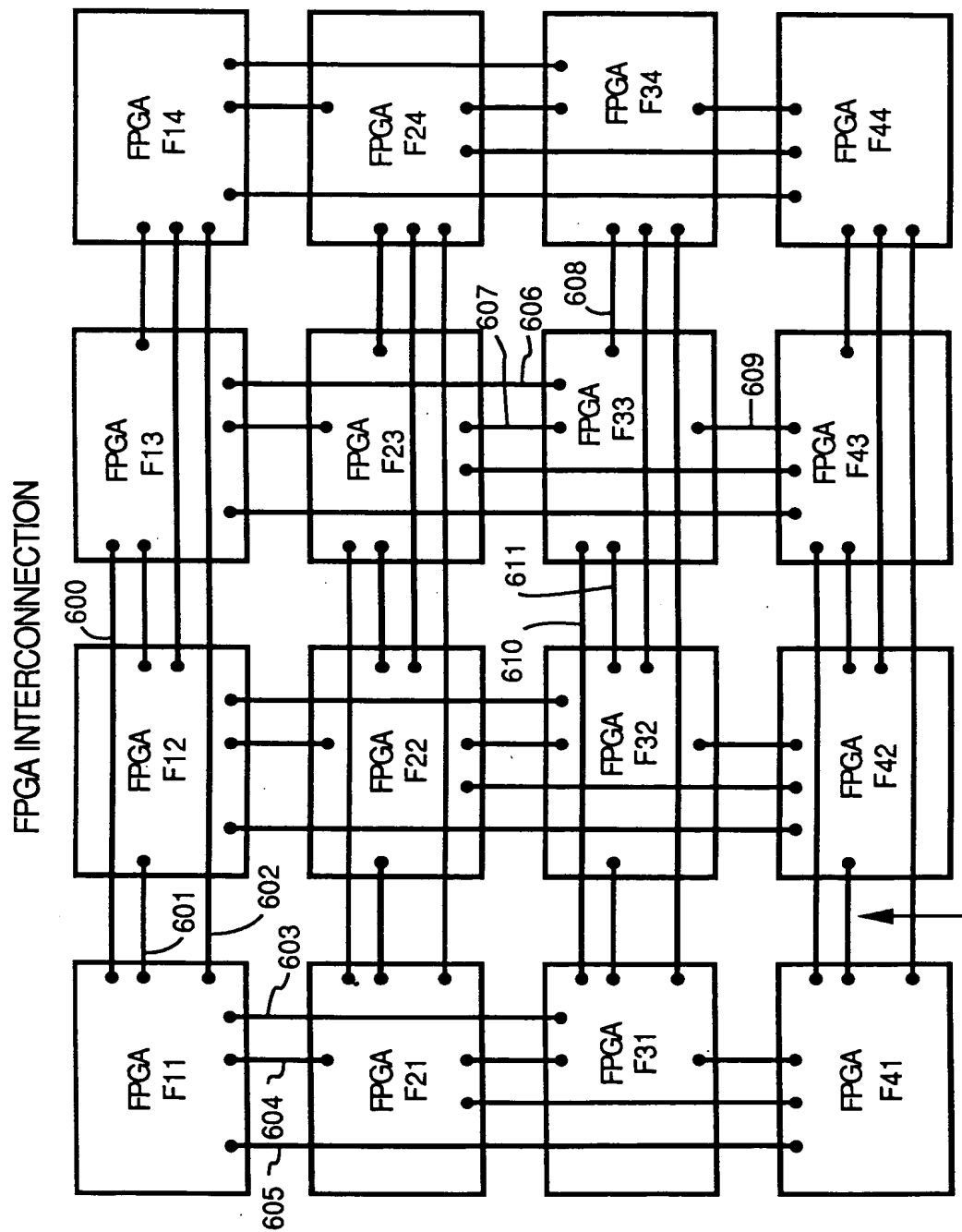


FIG. 8

1/6 of total I/O pins of FPGA for interconnection

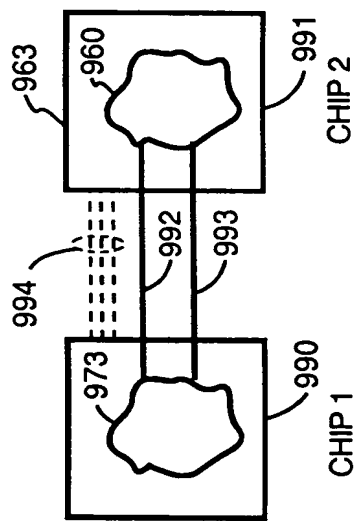


FIG. 9(a)

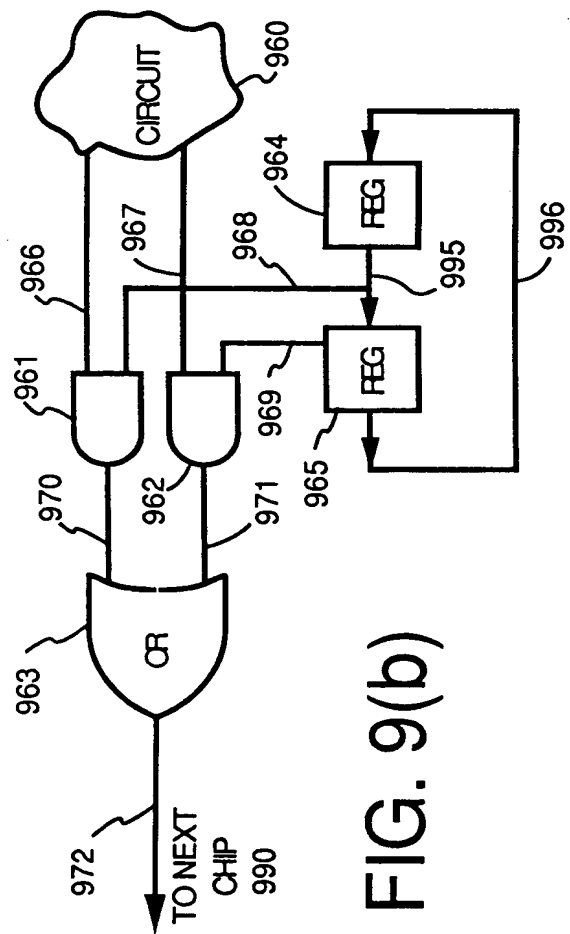


FIG. 9(b)



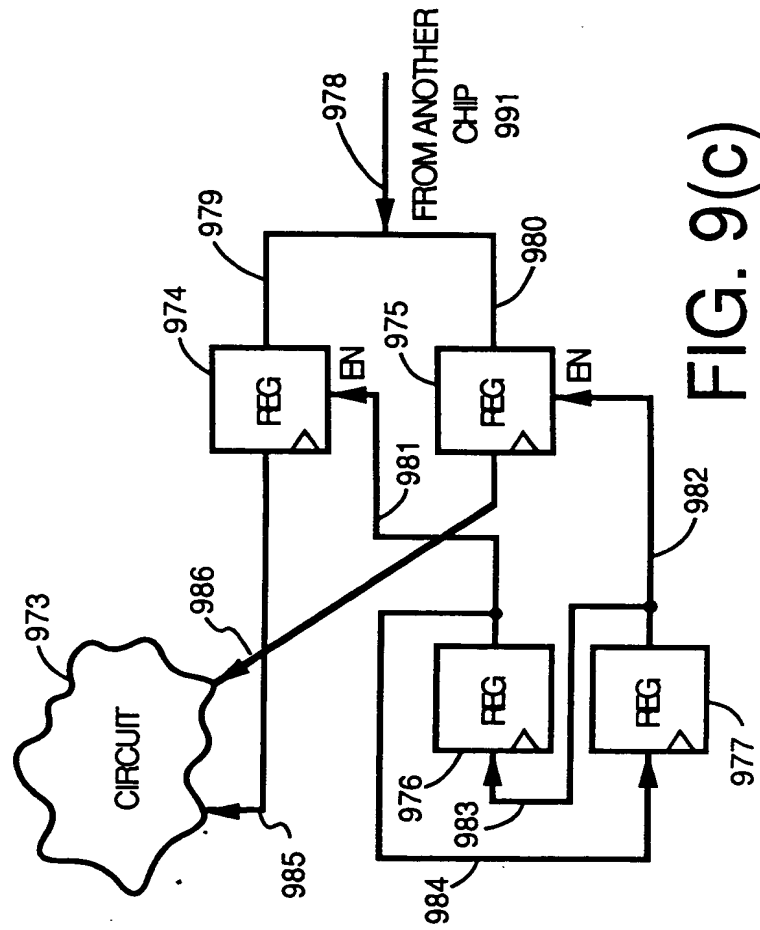
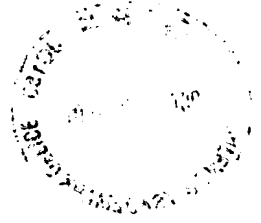


FIG. 9(c)



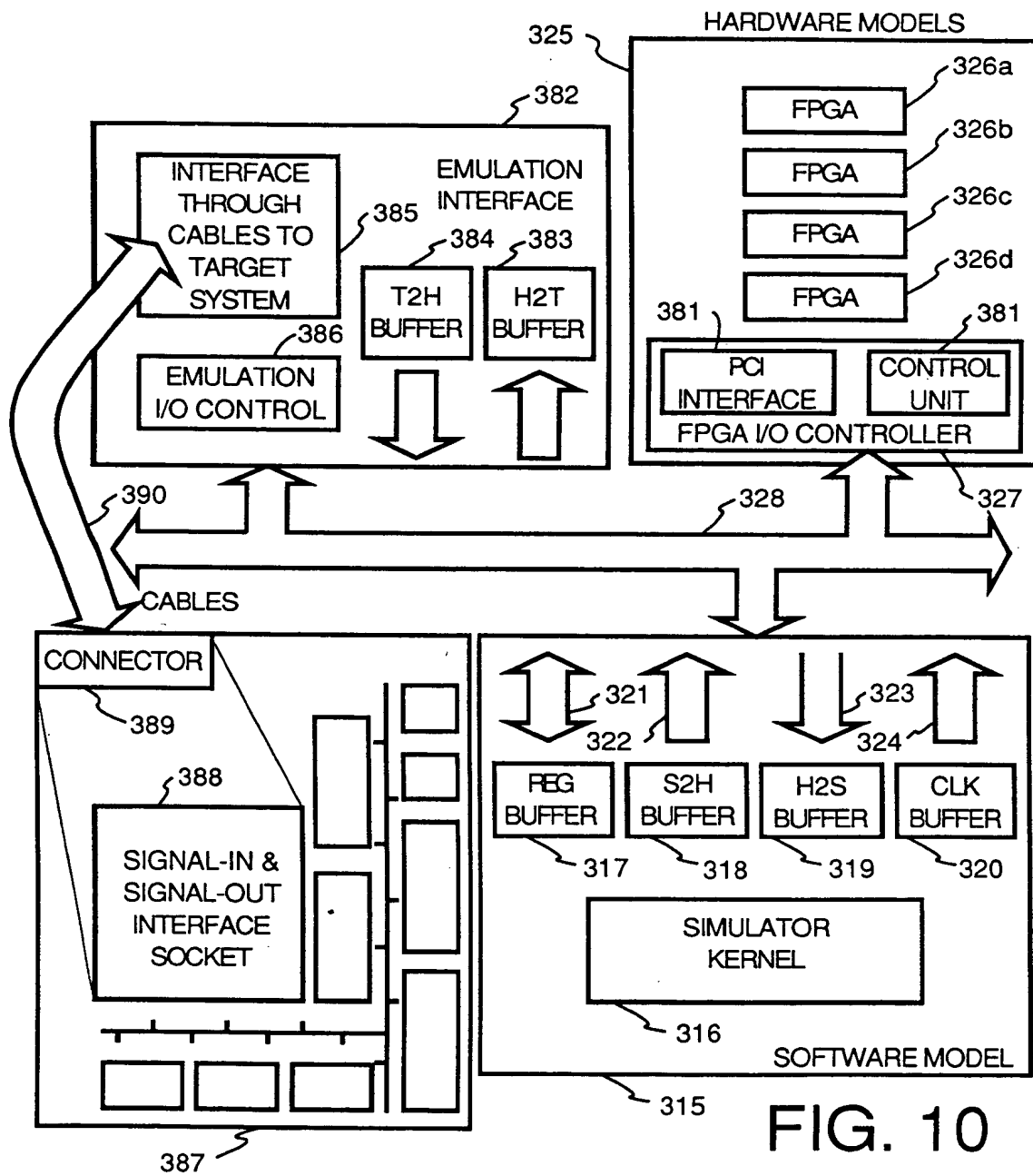


FIG. 10

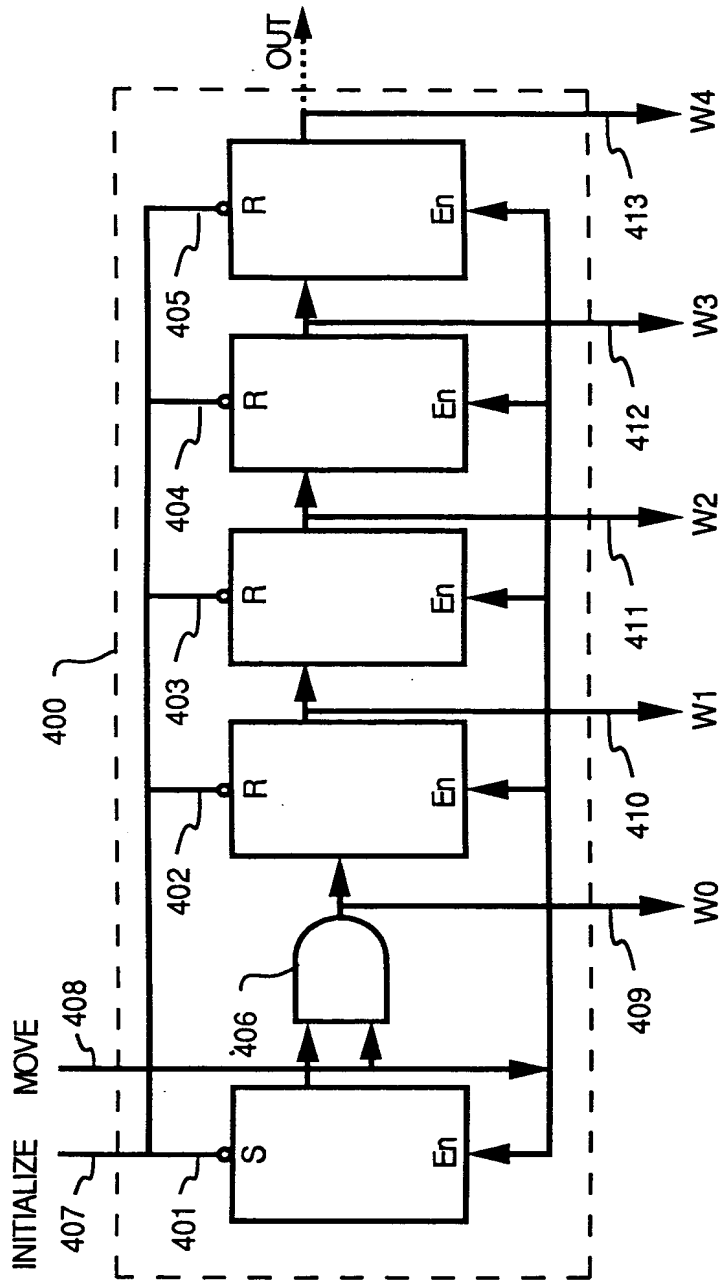
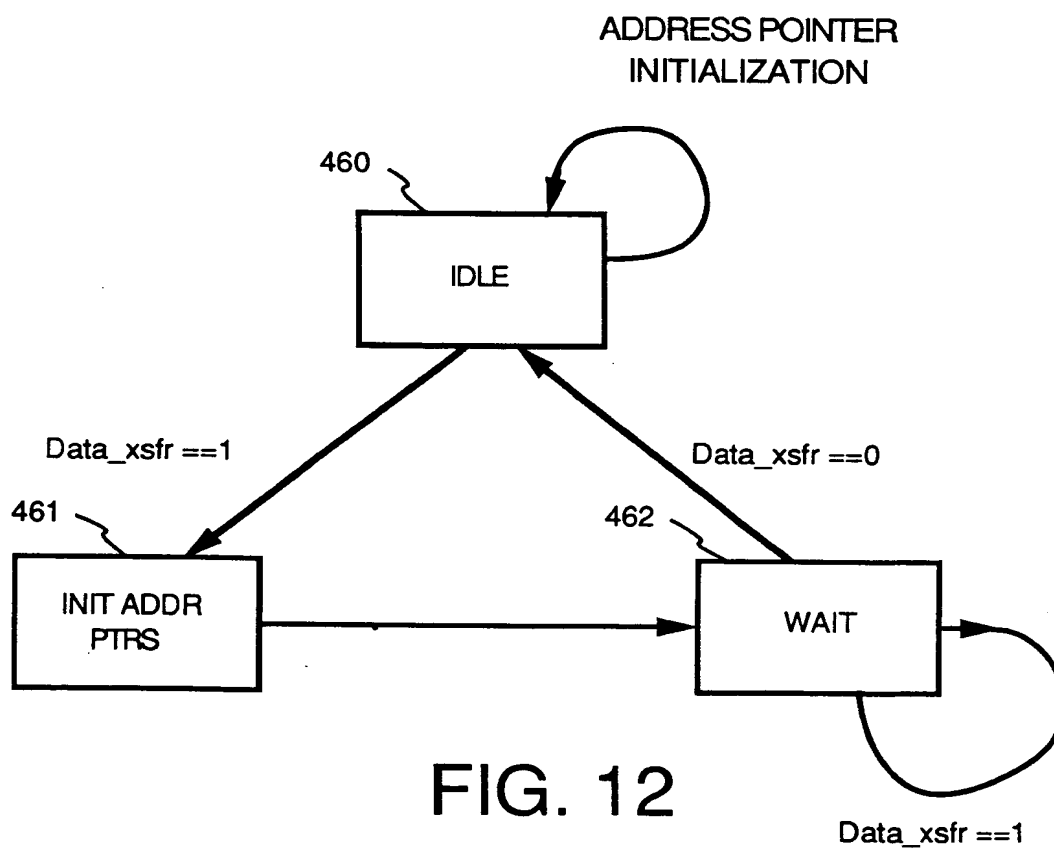


FIG. 11





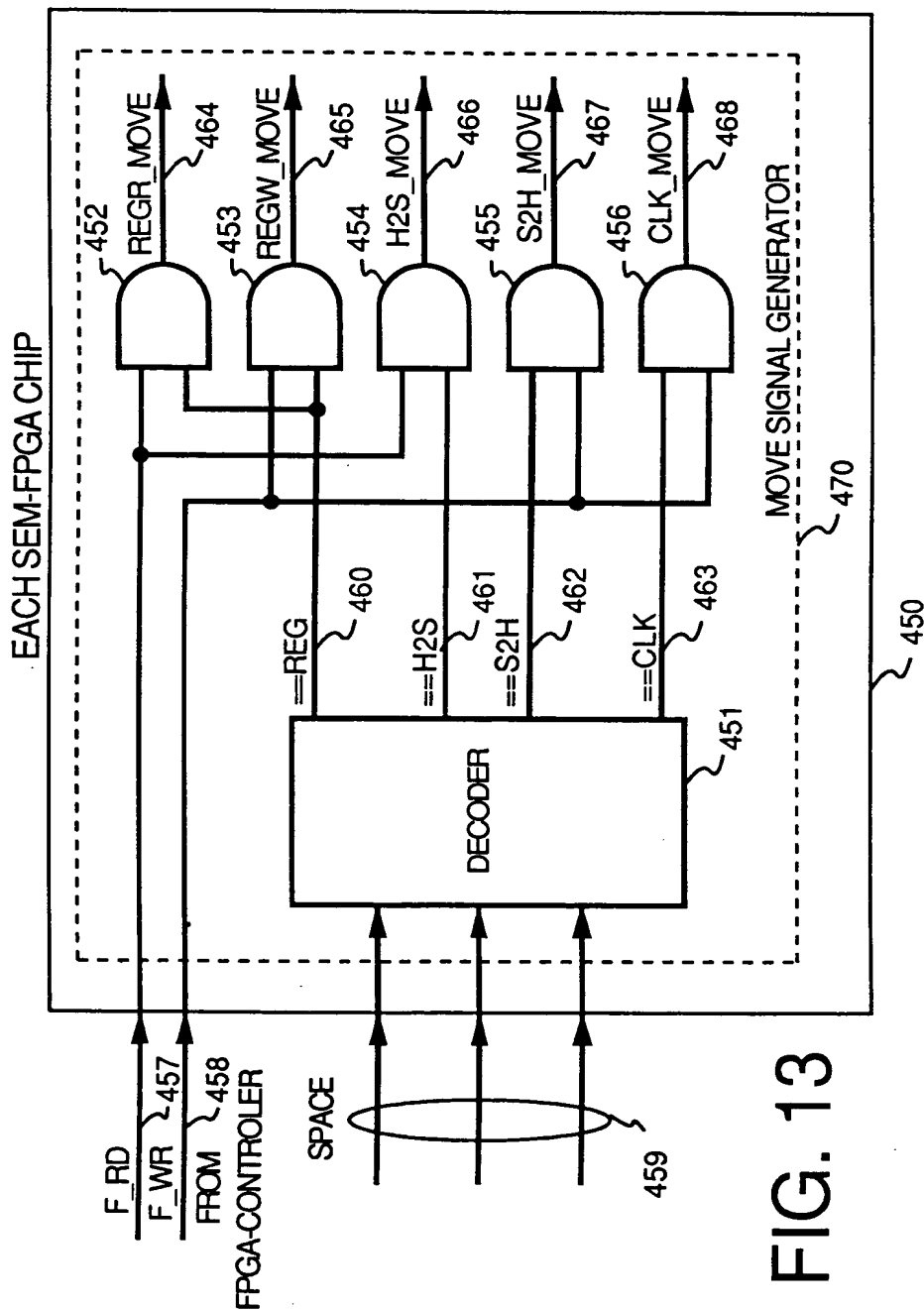


FIG. 13



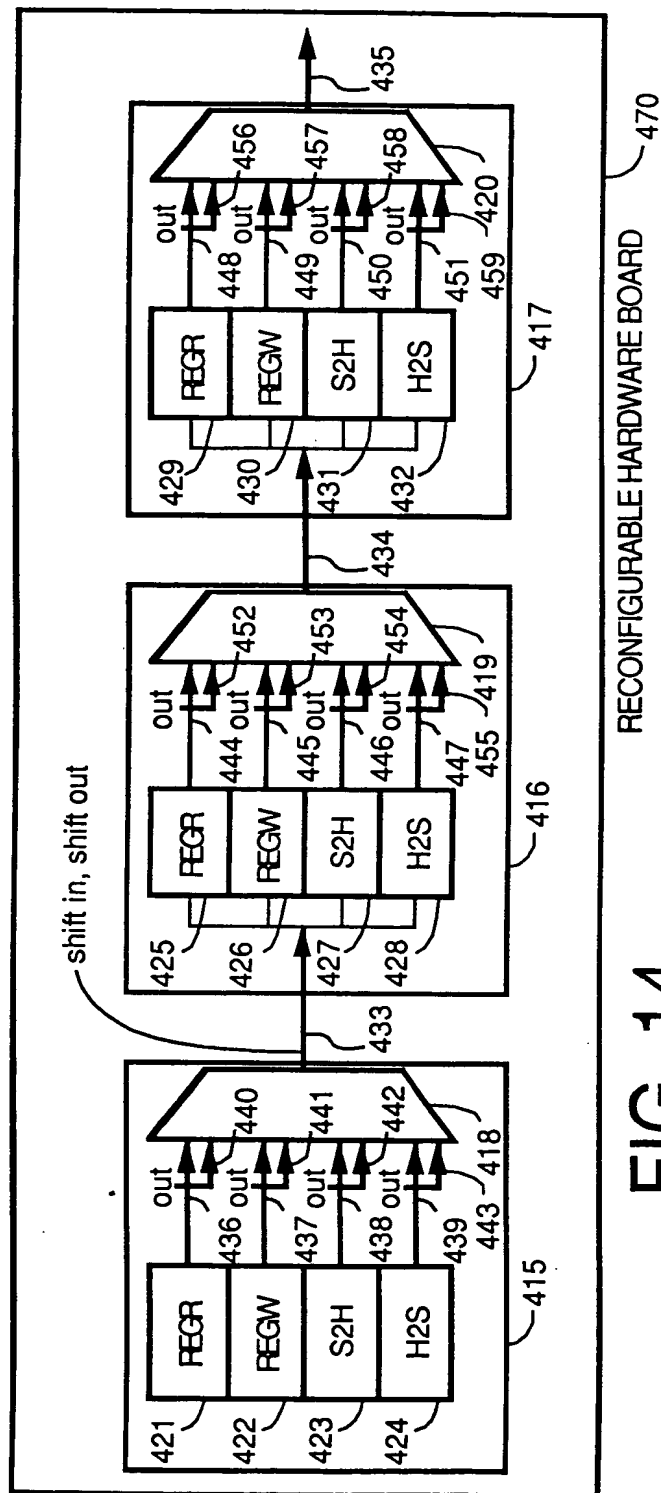


FIG. 14



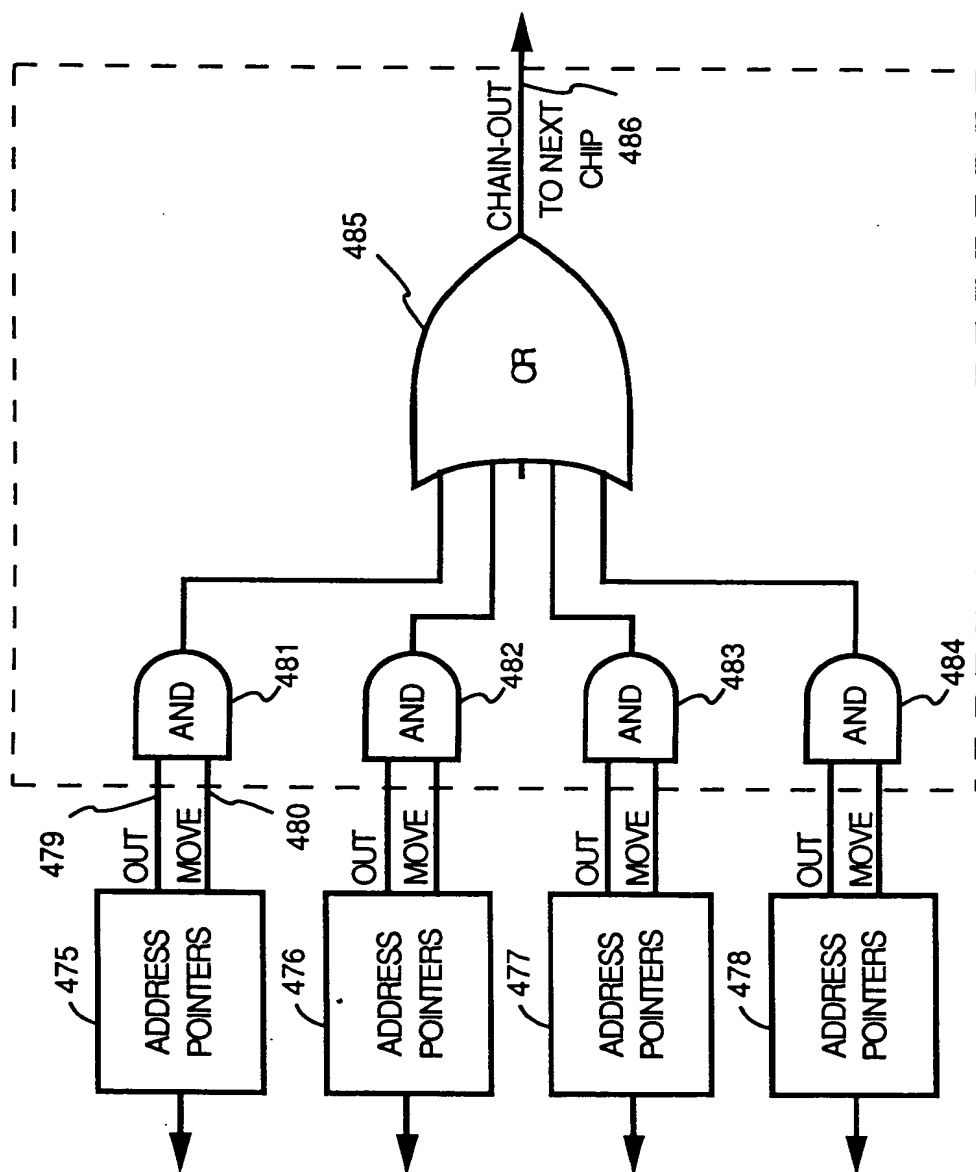


FIG. 15



FOOTNOT 10100660

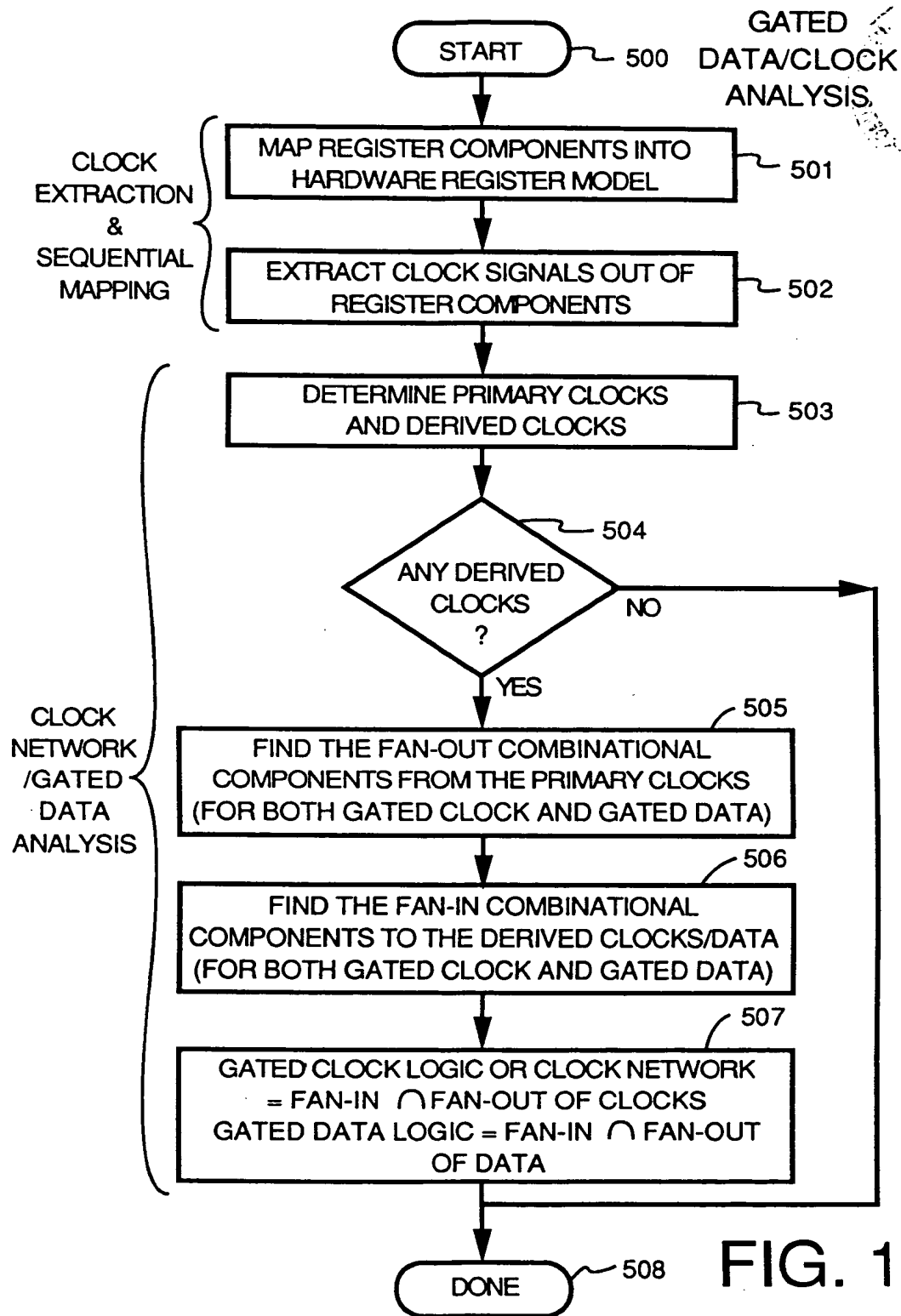


FIG. 16

FOOT" 42E00650

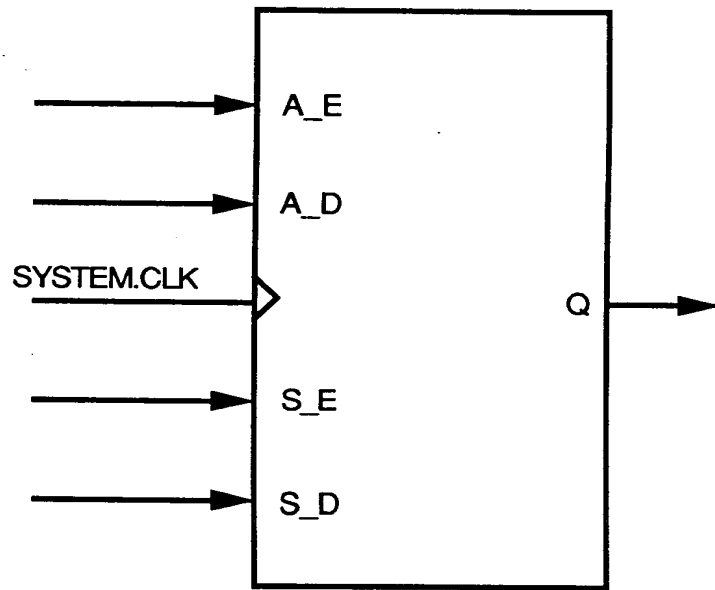


FIG. 17

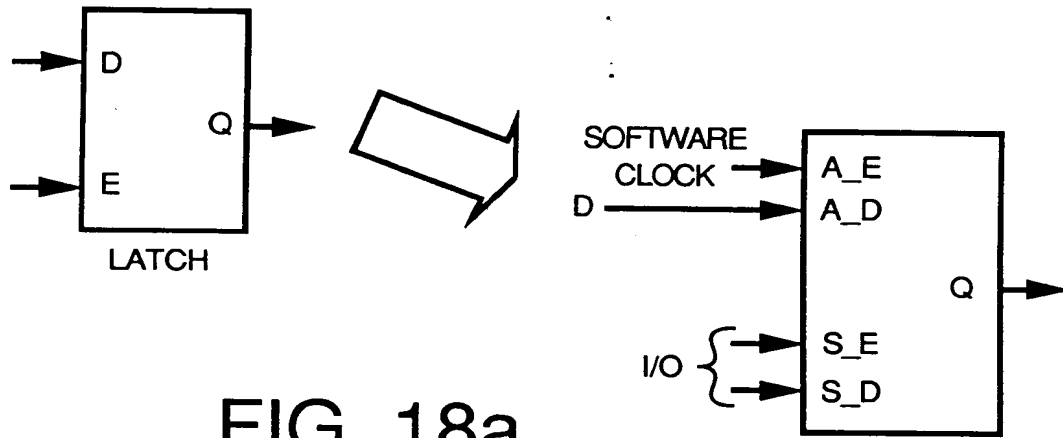


FIG. 18a

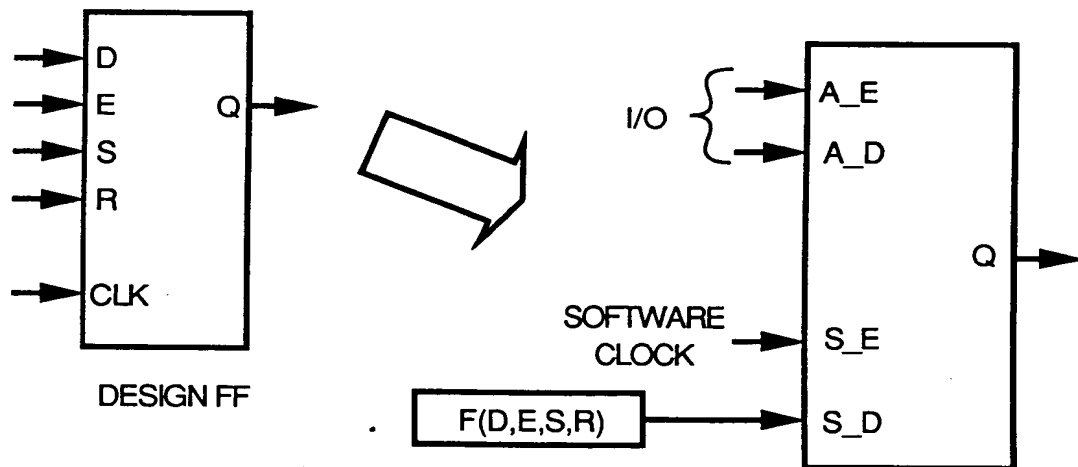


FIG. 18b

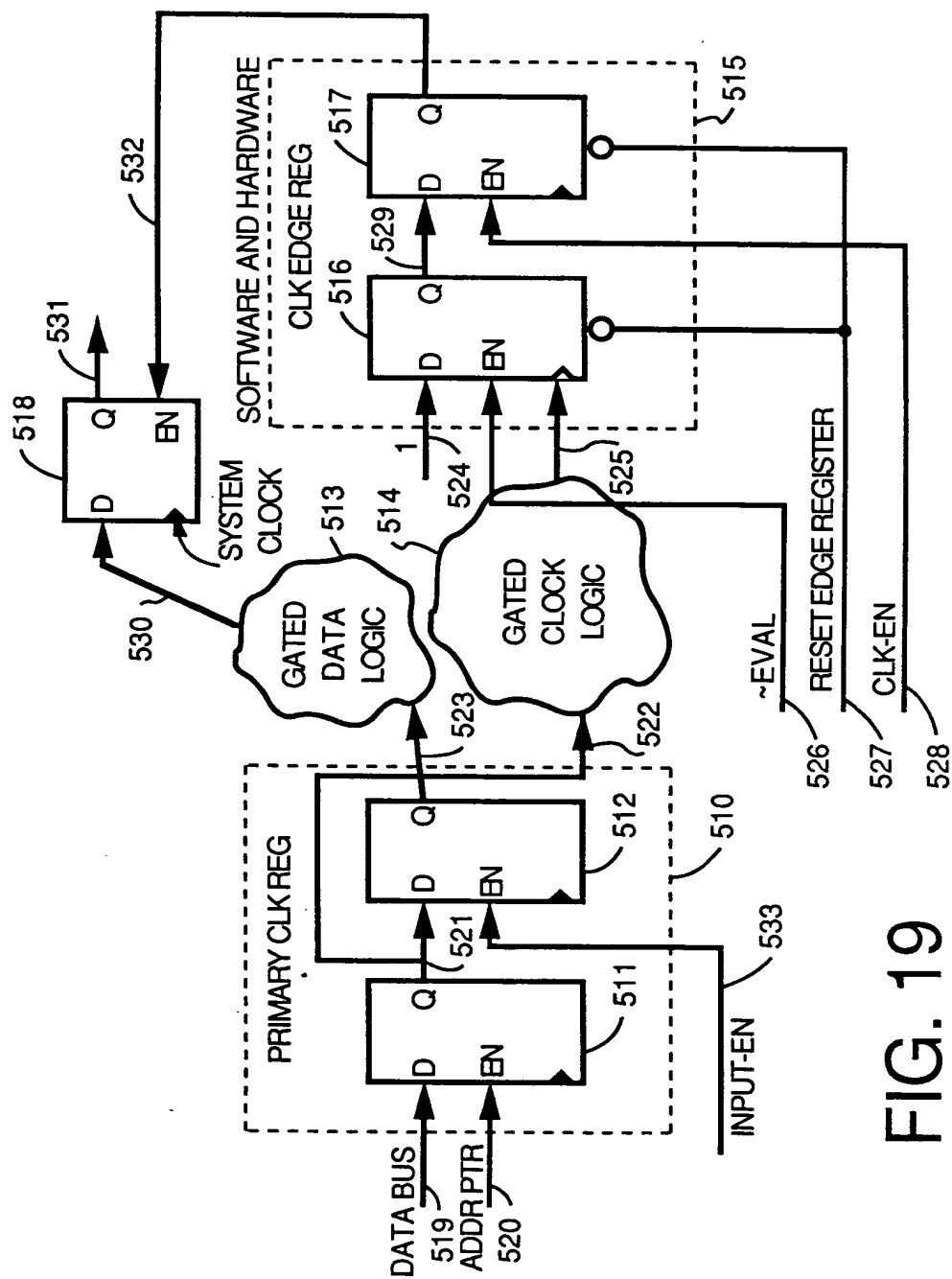


FIG. 19

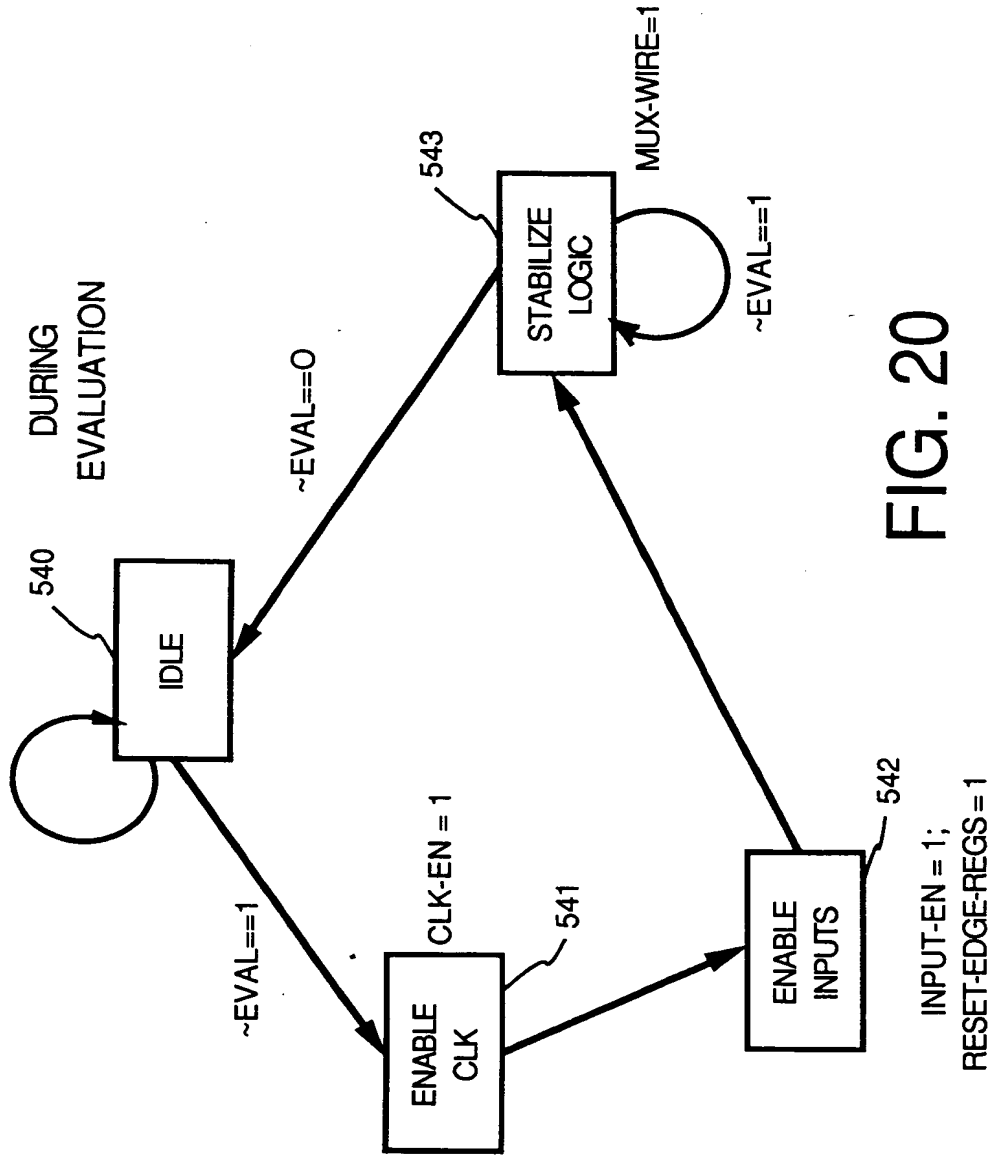


FIG. 20

TOPOT-42F00660

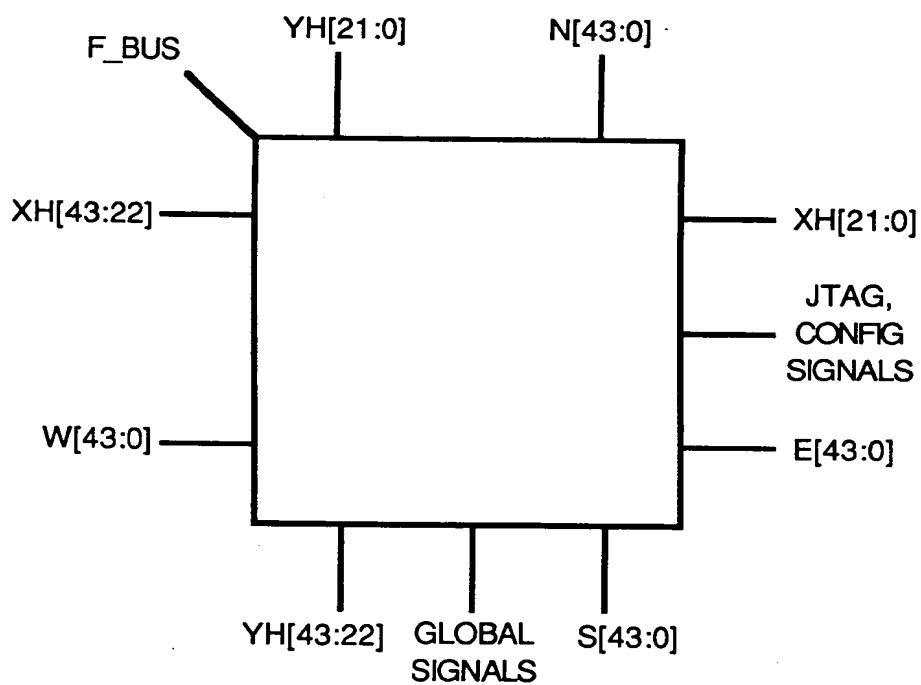
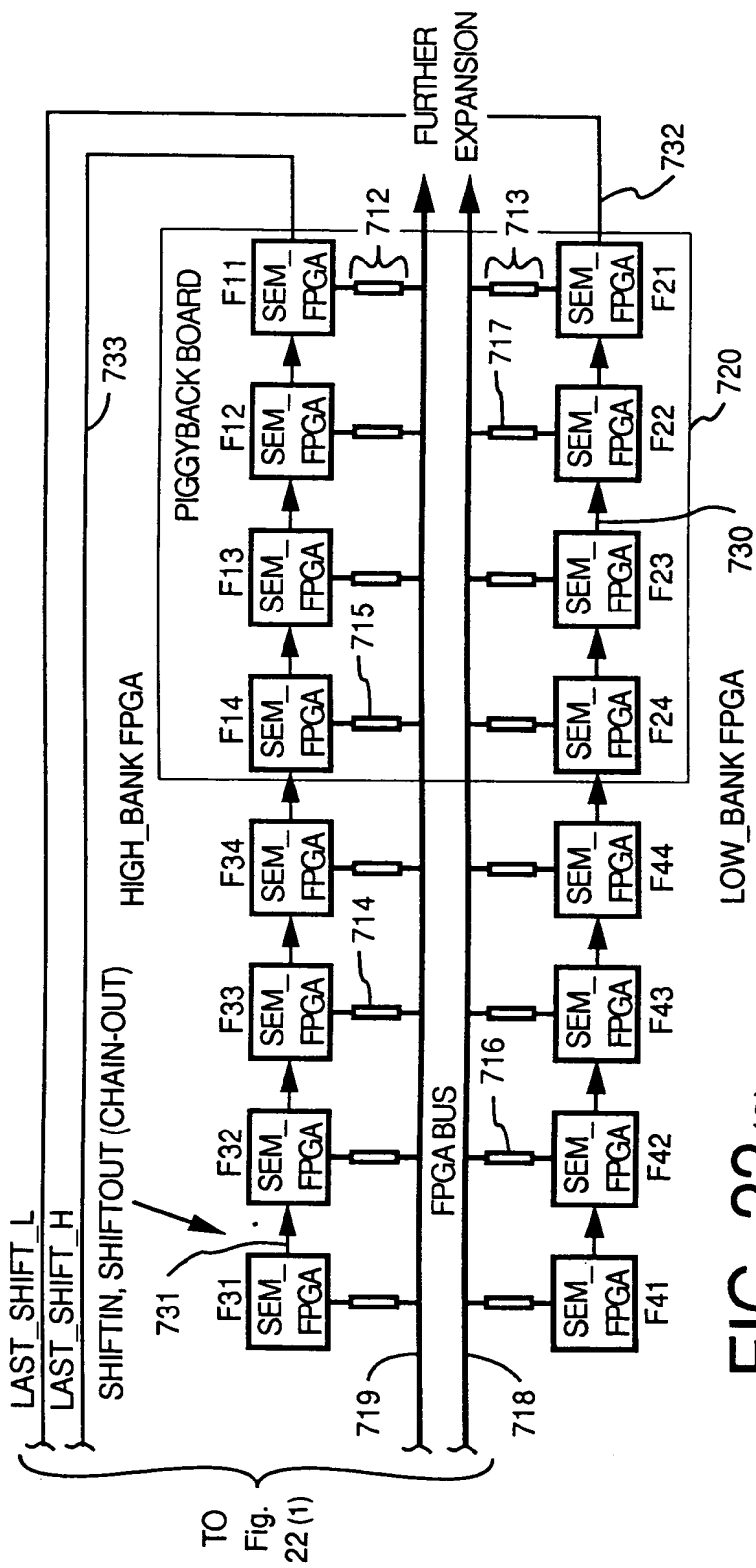


FIG. 21



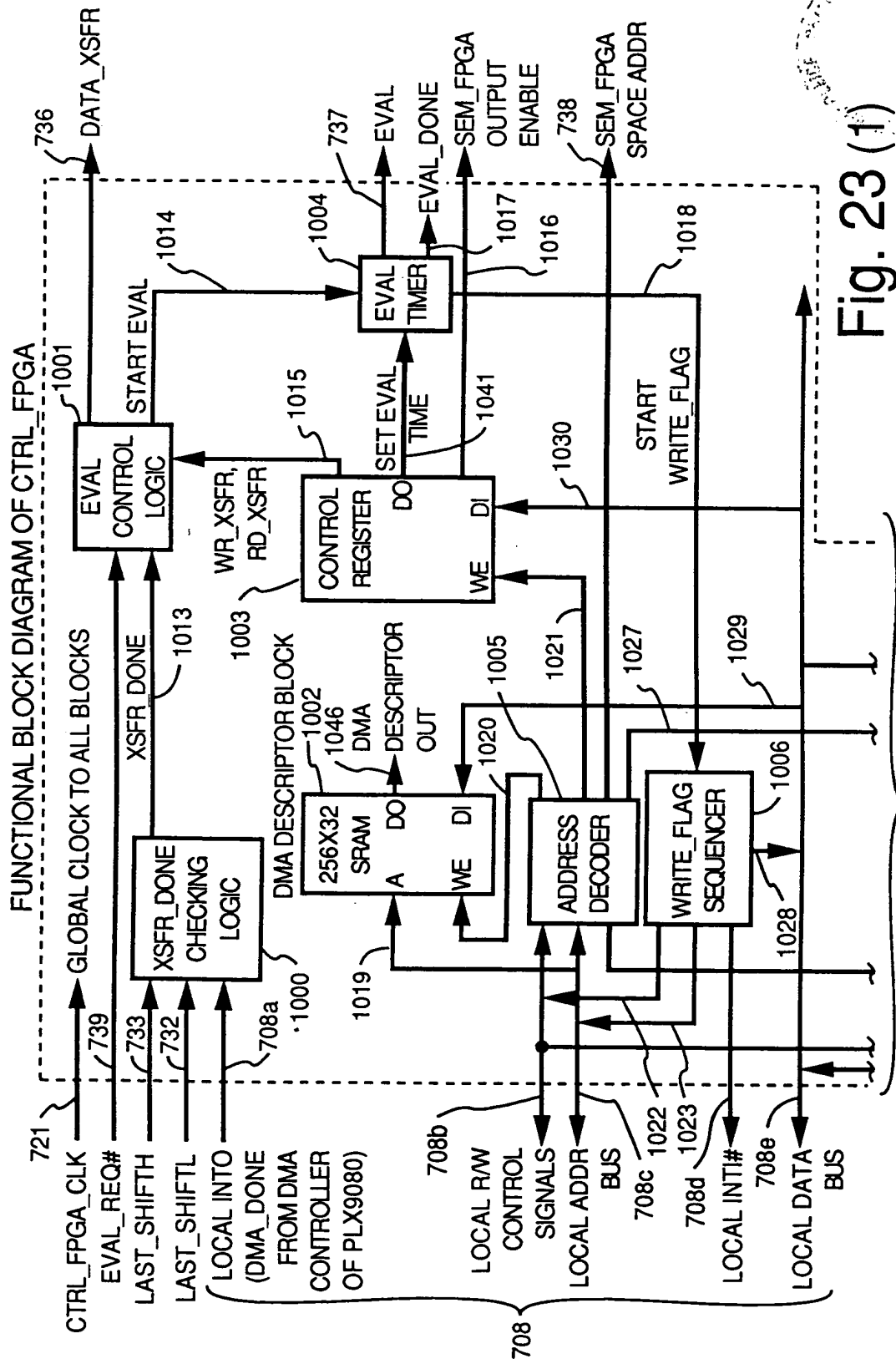


Fig. 23 (1)

To Fig. 23 (2)

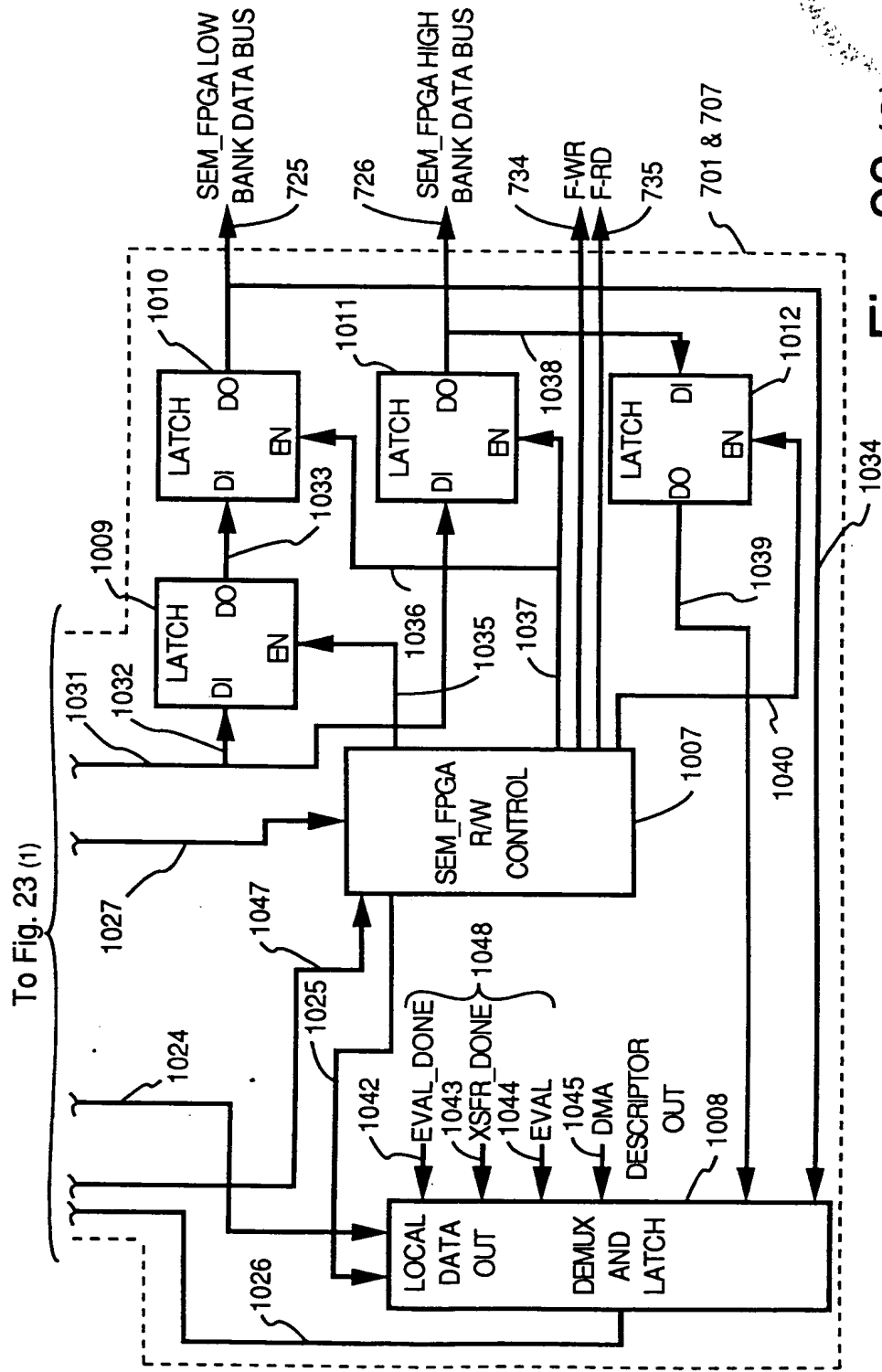


Fig. 23 (2)

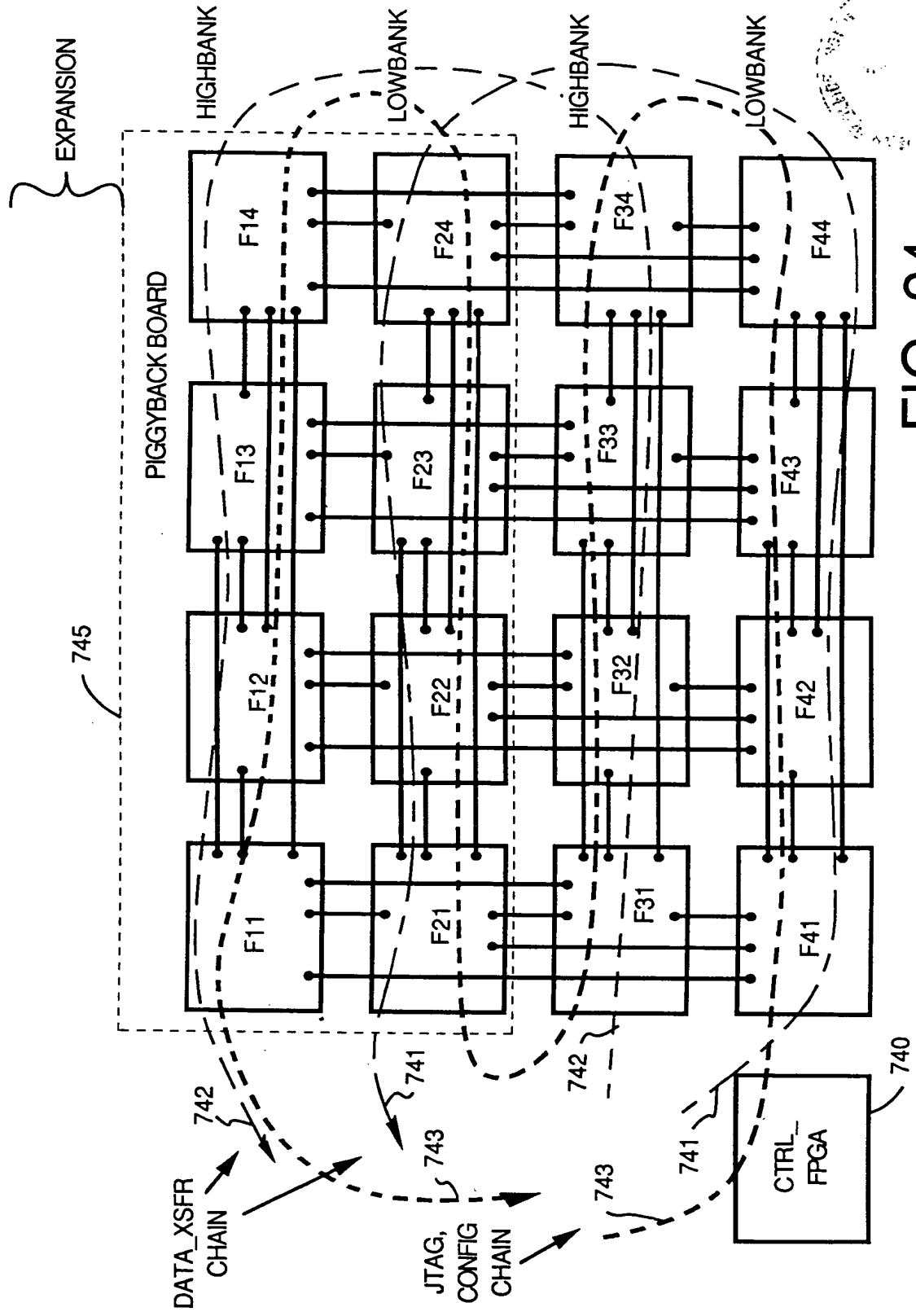


FIG. 24

000014-101001

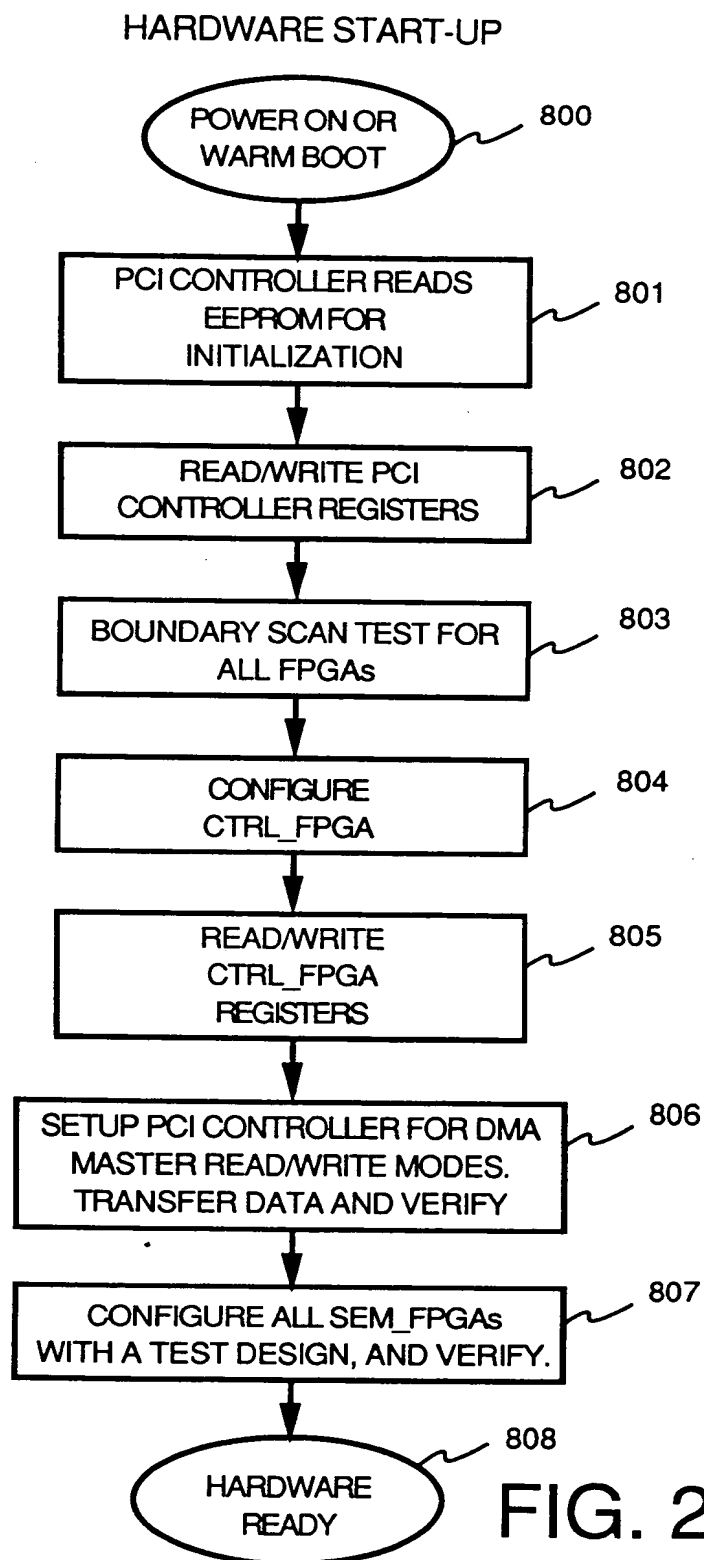


FIG. 25

```

module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(posedge clock or negedge reset)
    if(~reset)
        q = 0;
    else
        q = d;
endmodule

module example;
    wire d1, d2, d3;
    wire q1, q2, q3;
    reg signin;
    wire sigout;
    reg clk, reset;

    register reg1 (clk, reset, d1, q1);
    register reg2 (clk, reset, d2, q2);
    register reg3 (clk, reset, d3, q3);

    assign d1 = signin ^ q3;
    assign d2 = q1 ^ q3;
    assign d3 = q2 ^ q3;
    assign sigout = q3;

    // a clock generator
    always
    begin
        clk = 0;
        #5;
        clk = 1;
        #5;
    end

    // a signal generator
    always
    begin
        #10;
        signin = $random;
    end

    // initialization
    initial
    begin
        reset = 0;
        signin = 0;
        #1;
        reset = 1;
        #5;
        $monitor($time, " %b, %b", signin, sigout);
        #1000 $finish;
    end
end module

```

Fig. 26

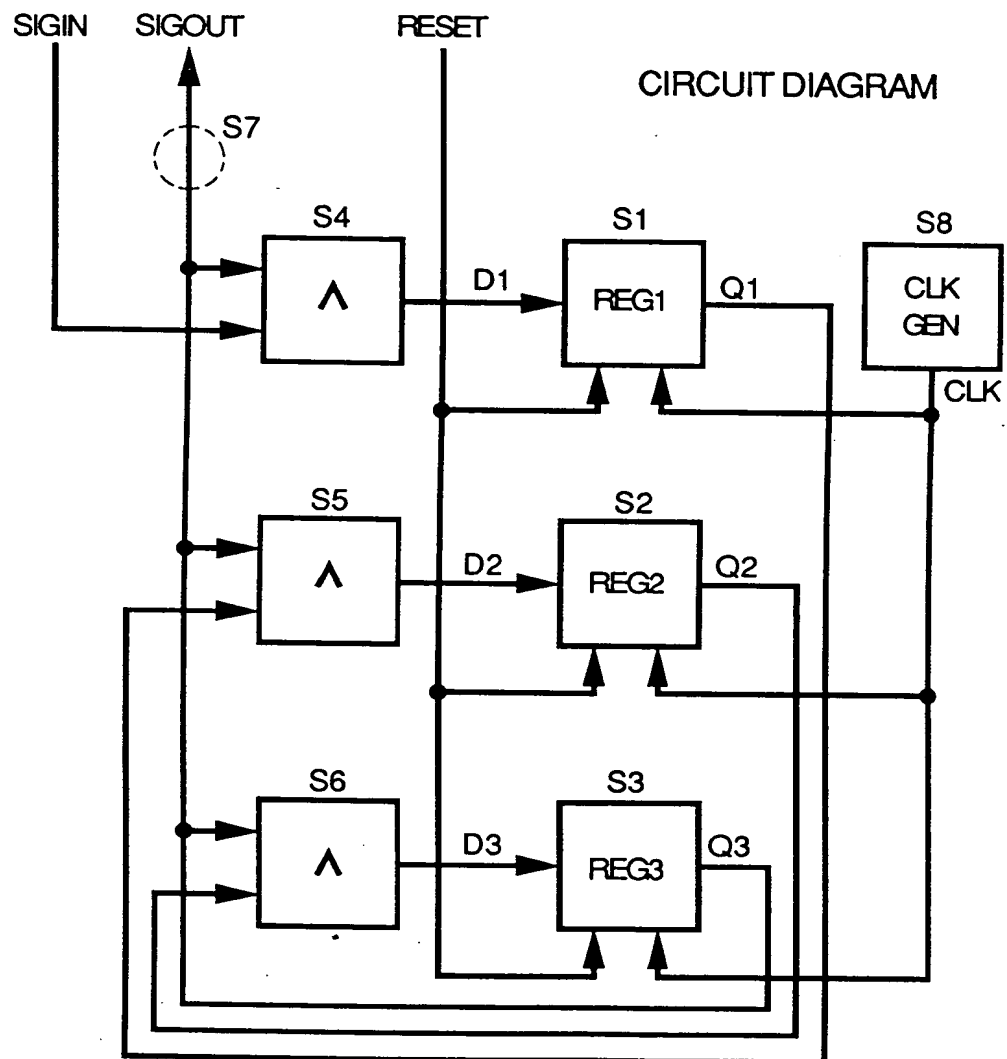


FIG. 27

```

module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

```

```

always@(post edge clock or negedge reset)
  if(~reset)
    q = 0
  else
    q = d;

```

```

endmodule

```

Register definition

900

```

module example;

```

```

  wire d1, d2, d3;

```

```

  wire q1, q2, q3;

```

Wire interconnection info

907

```

  reg sign;

```

Test-bench input -- 908

```

  wire sigout;

```

Test-bench output -- 909

```

  reg clk, reset;

```

```

S1 register reg 1 (clk, reset, d1, q1);

```

```

S2 register reg 2 (clk, reset, d2, q2);

```

```

S3 register reg 3 (clk, reset, d3, q3);

```

Register component

901

```

S4 assign d1 = sign ^ q3;

```

```

S5 assign d2 = q1 ^ 3;

```

```

S6 assign d3 = q2 ^ q3;

```

```

S7 assign signout = q3;

```

Combinational component

902

S8

```

  // a clock generator
  always

```

```

  begin

```

```

    clk = 0;

```

```

    #5;

```

```

    clk = 1;

```

```

    #5;

```

```

  end

```

Clock component

903

S9

```

  // a signal generator
  always

```

```

  begin

```

```

    #10;

```

```

    sign = $random;

```

```

  end

```

Test-bench component (Driver)

904

```

  // initialization
  initial

```

```

  begin

```

```

    reset = 0;

```

```

    sign = 0;

```

```

    #1;

```

```

    reset = 1;

```

```

    #5;

```

```

    $monitor($time, "%b, %b", sign, sigout);

```

```

    #1000 $finish;

```

```

  end

```

```

end module

```

Test-bench component (initialization)

905

Test-bench

component

(monitor)

906

Fig. 28

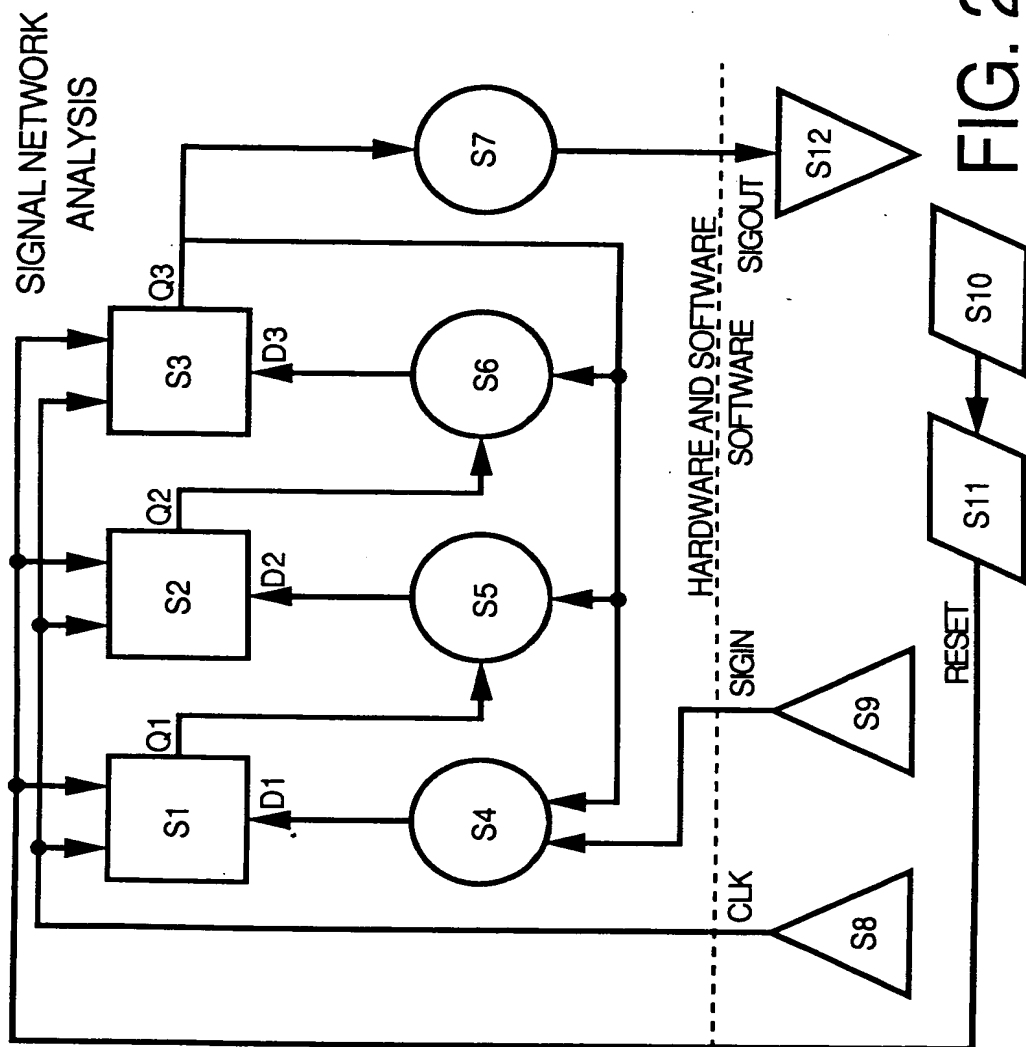
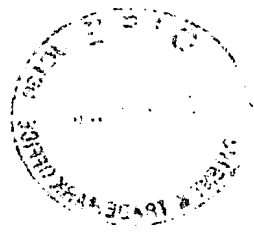


FIG. 29



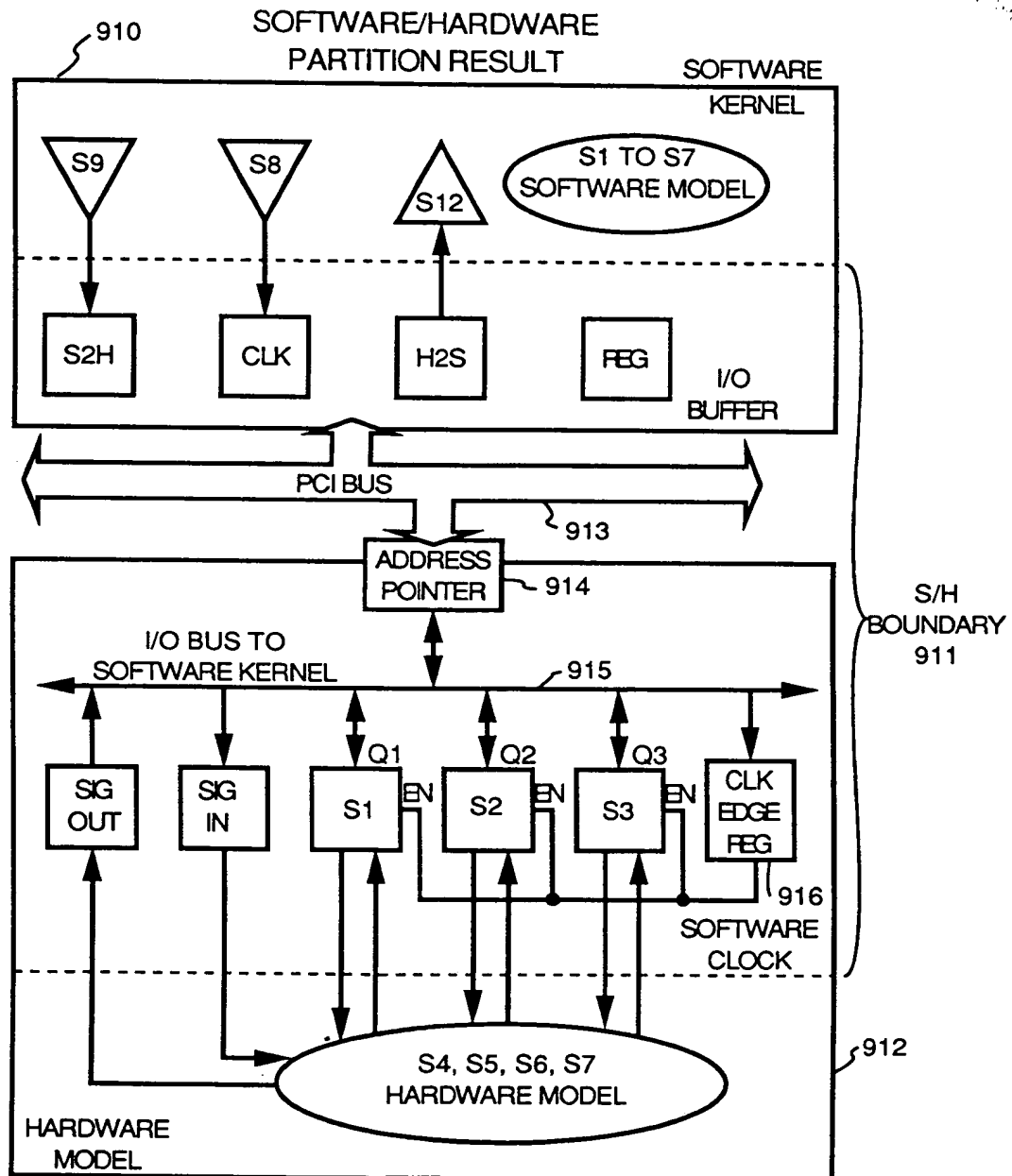


FIG. 30

HARDWARE MODEL

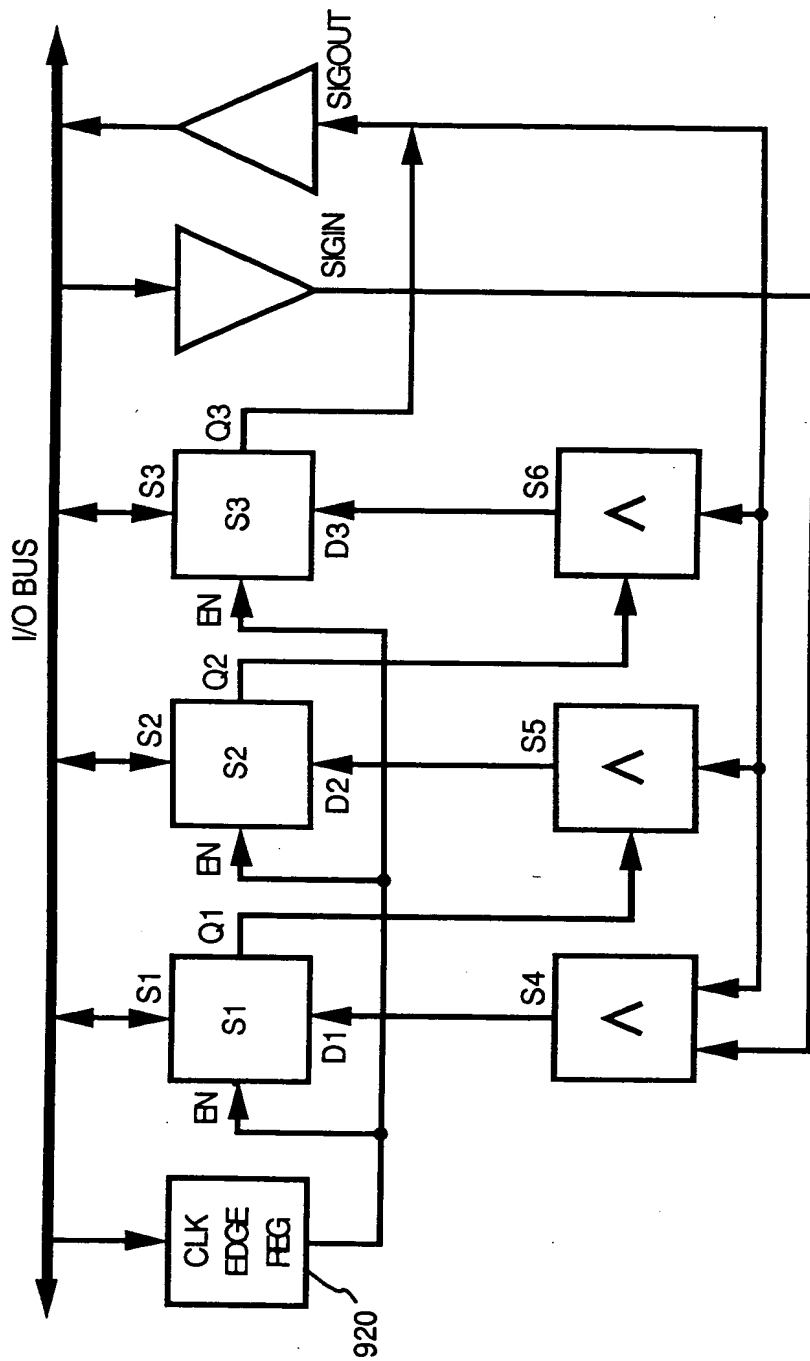


FIG. 31

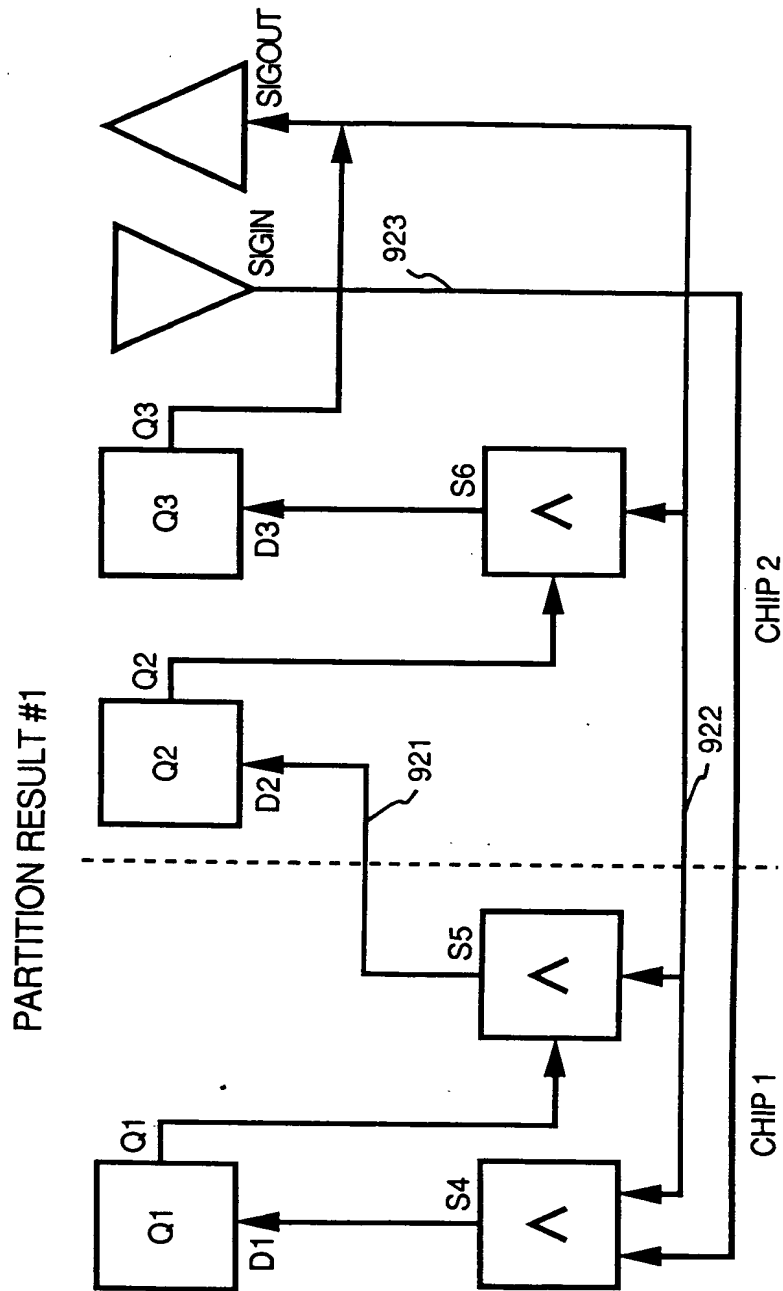


FIG. 32

(IGNORE I/O AND CLOCK EDGE REGISTER)



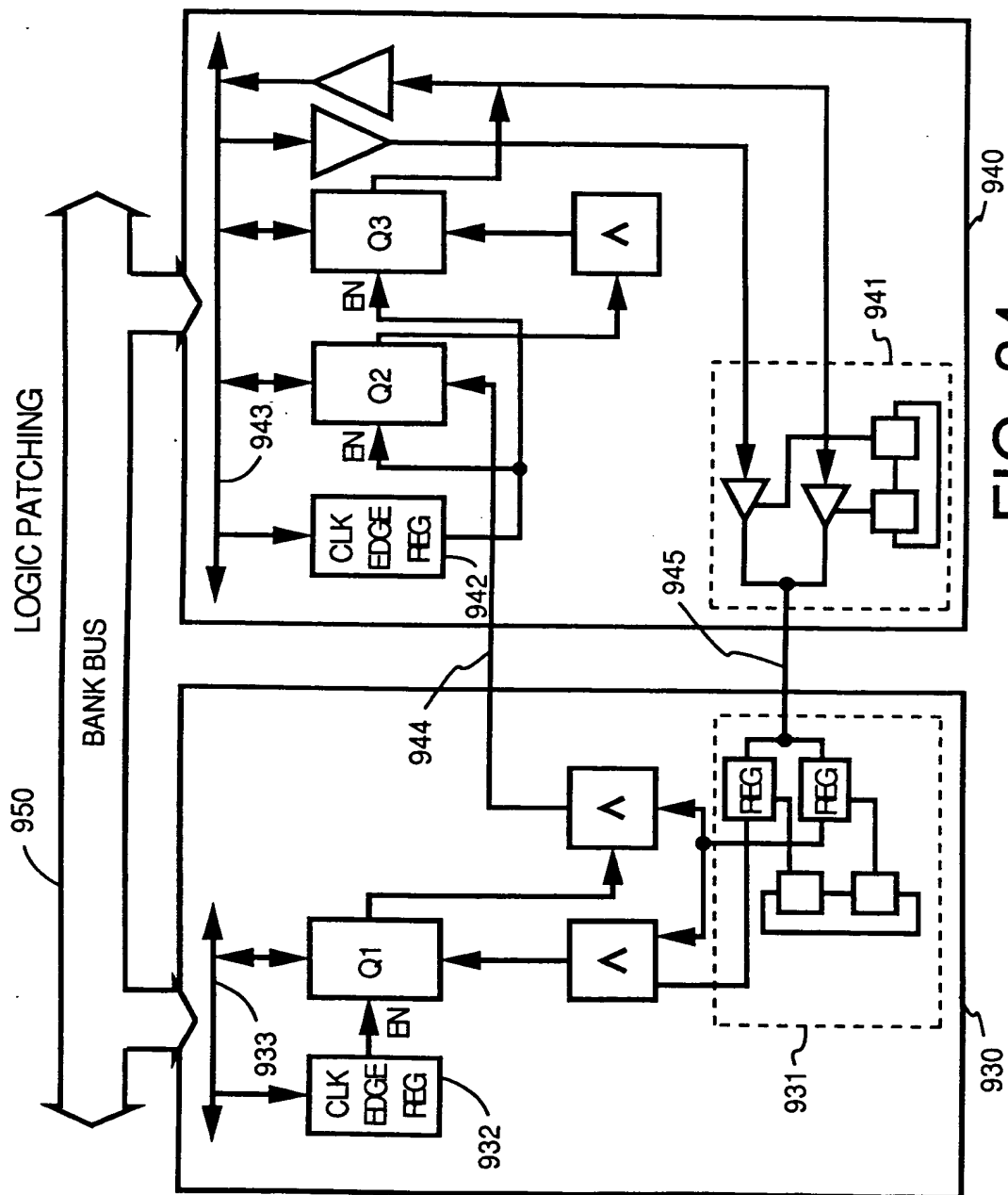


FIG. 34

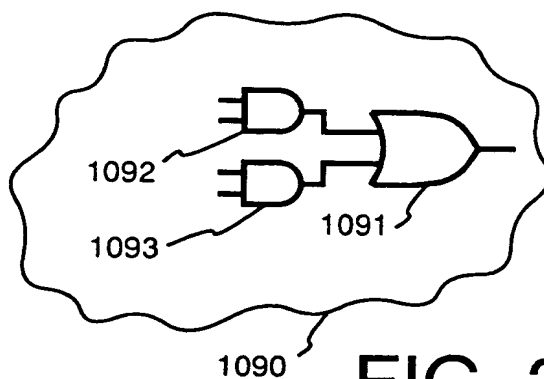


FIG. 35a

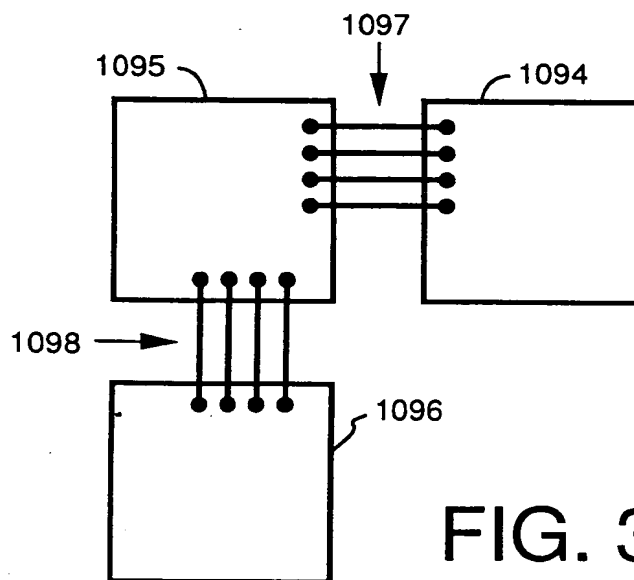


FIG. 35b

FIG. 35c

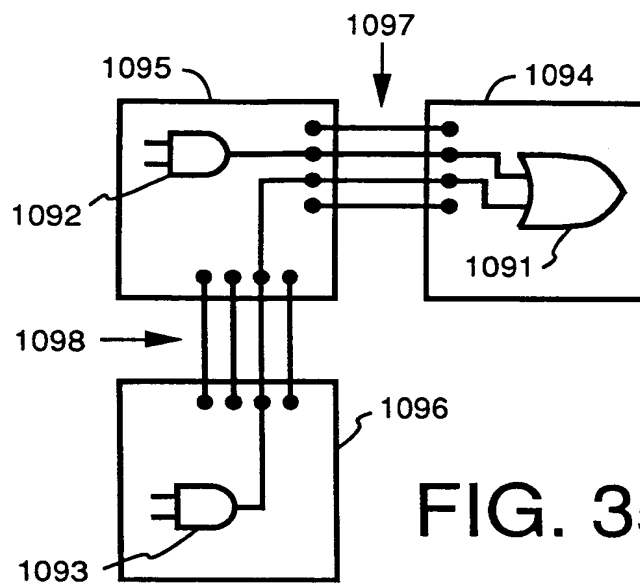


FIG. 35c

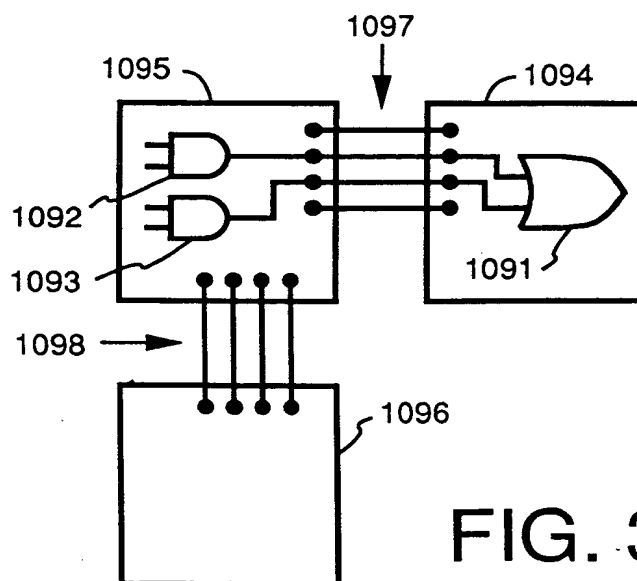


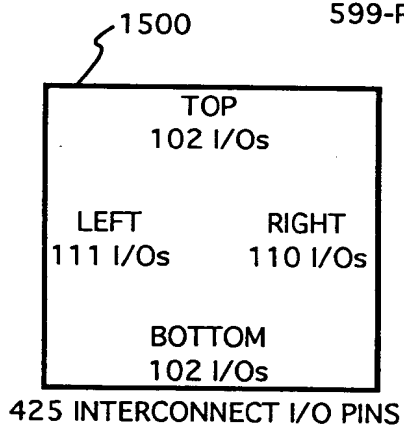
FIG. 35d

09900144-101001



I/O PIN OVERVIEW OF FPGA LOGIC DEVICE

FPGA : 10K130V, 10K250V WITH
599-PIN PGA PACKAGE



45 DEDICATED I/O PINS :

GCLK, FD_BUS[31..0], F_RD, F_WR,
DATAXSFR, SHIFTIN, SHIFTOUT,
SPACE[2..0], EVAL, EV_REQ_N,
DEV_OE, DEV_CLRN

FIG. 36

09500124 " 101001
T0001 " 12100660

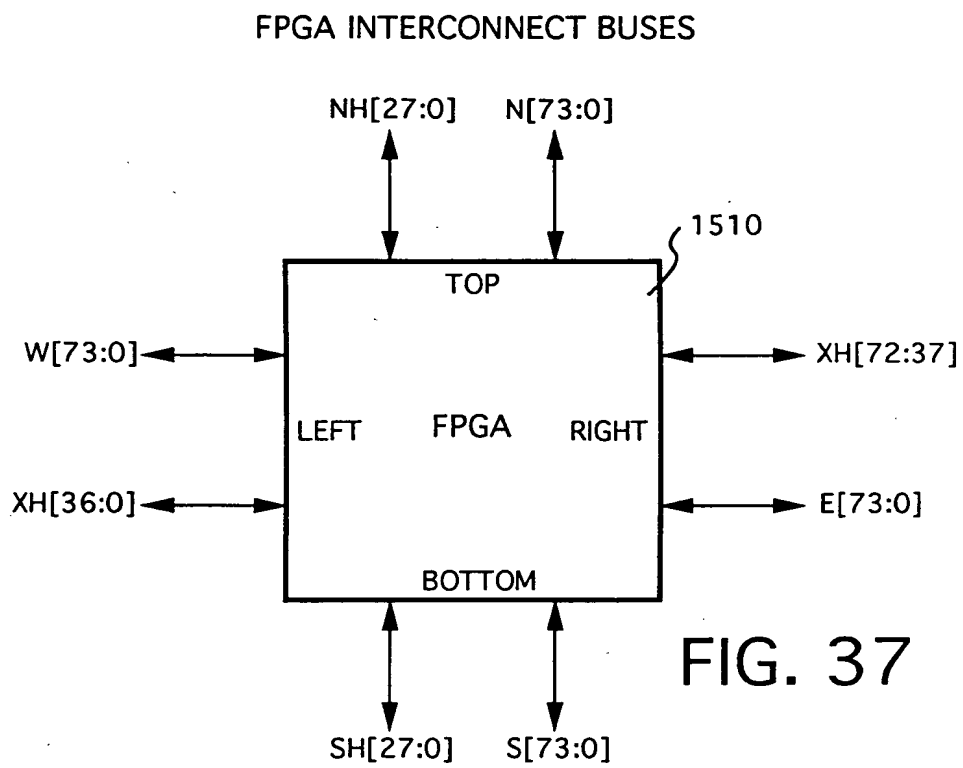


FIG. 37

SIX-BOARD CONFIGURATION DIRECT-NEIGHBOR AND ONE-HOP FPGA ARRAY-X TORUS, Y MESH

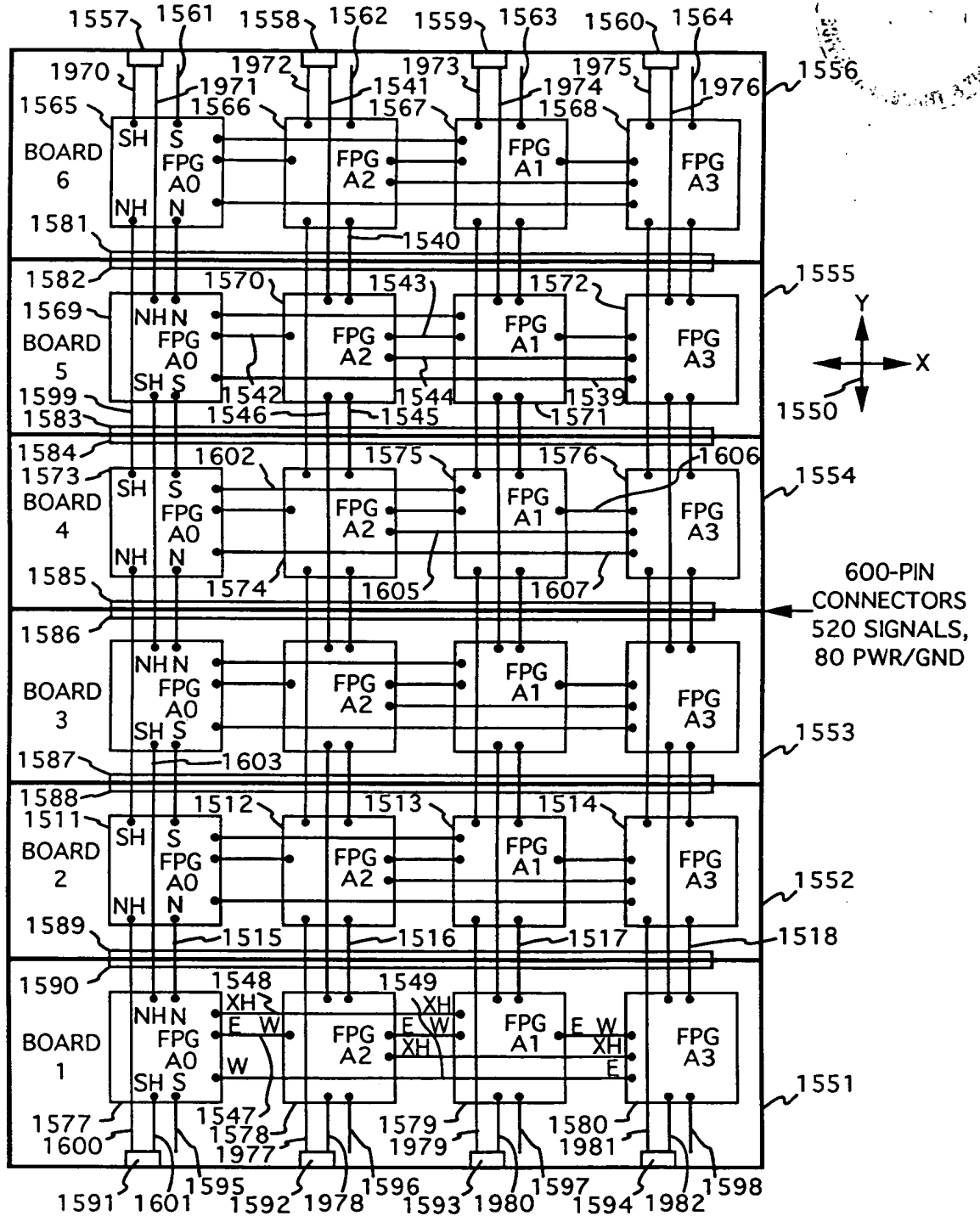


FIG. 39

FPGA ARRAY CONNECTION BETWEEN BOARDS

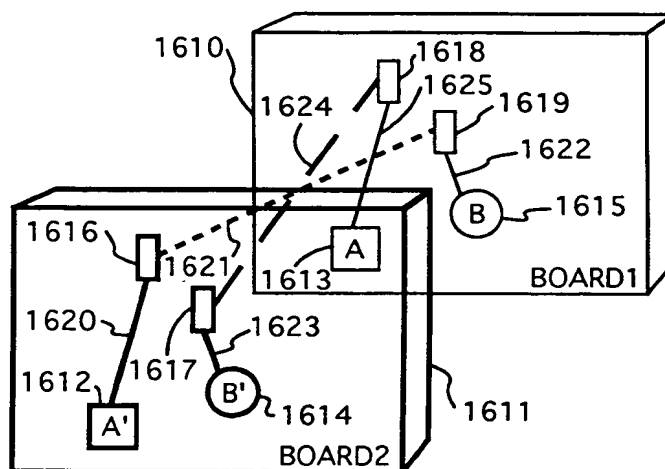


FIG. 40(a)

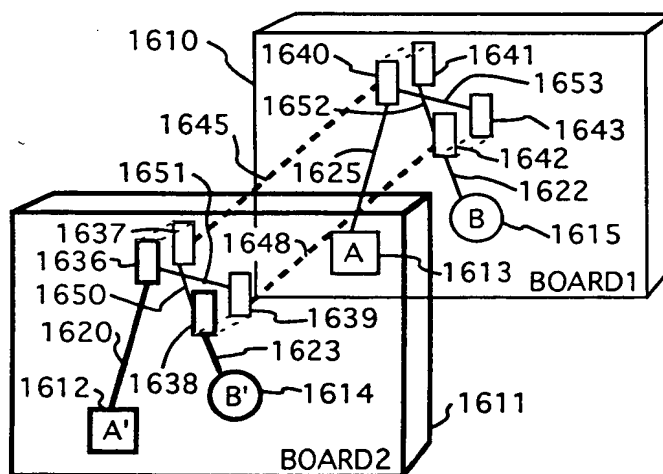
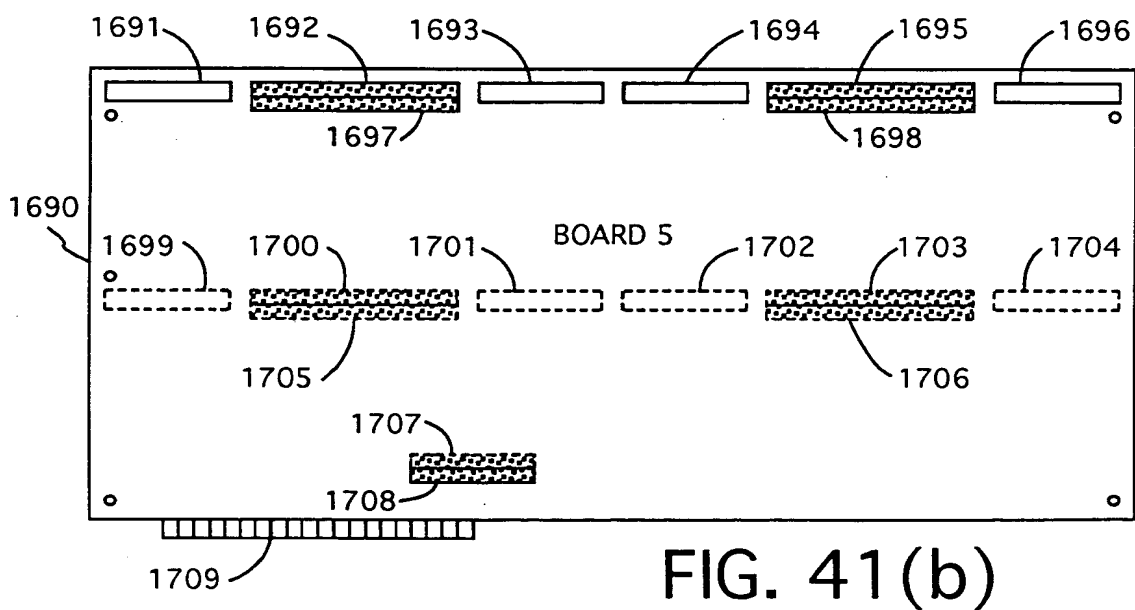
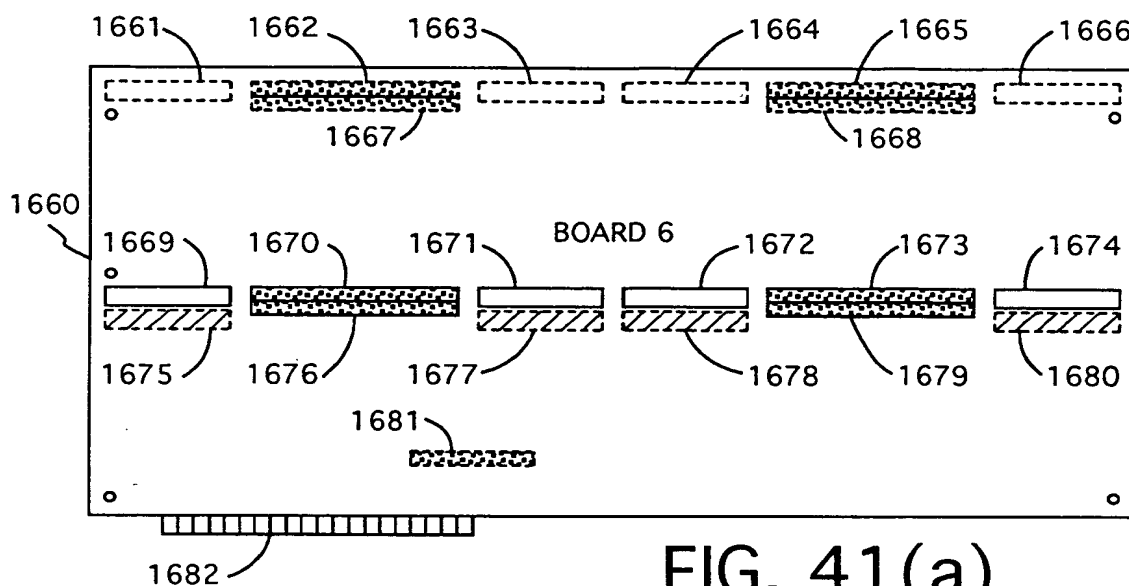
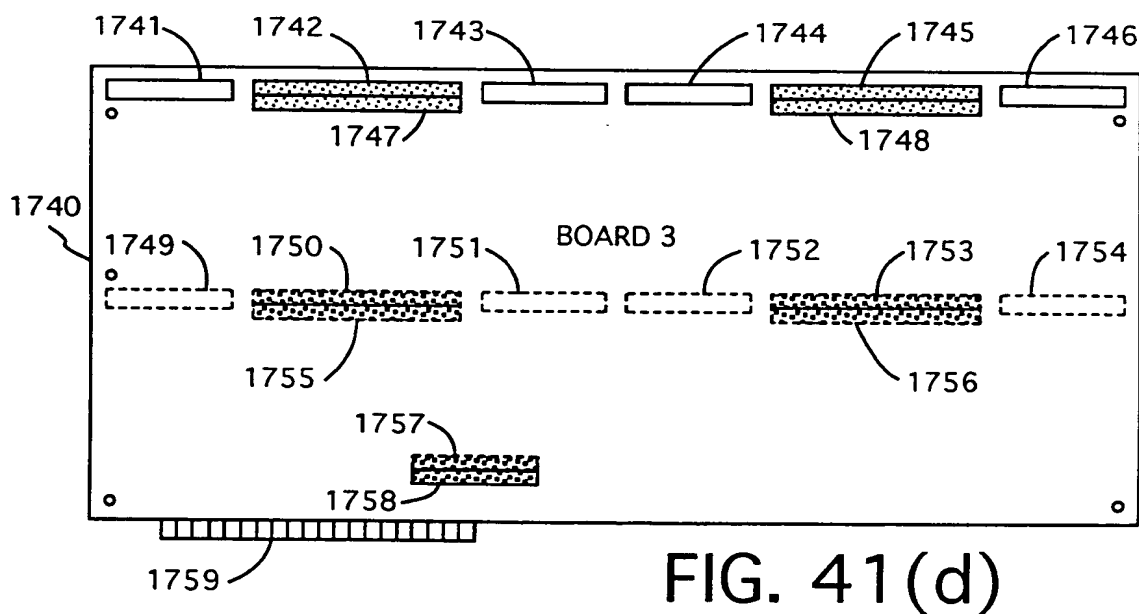
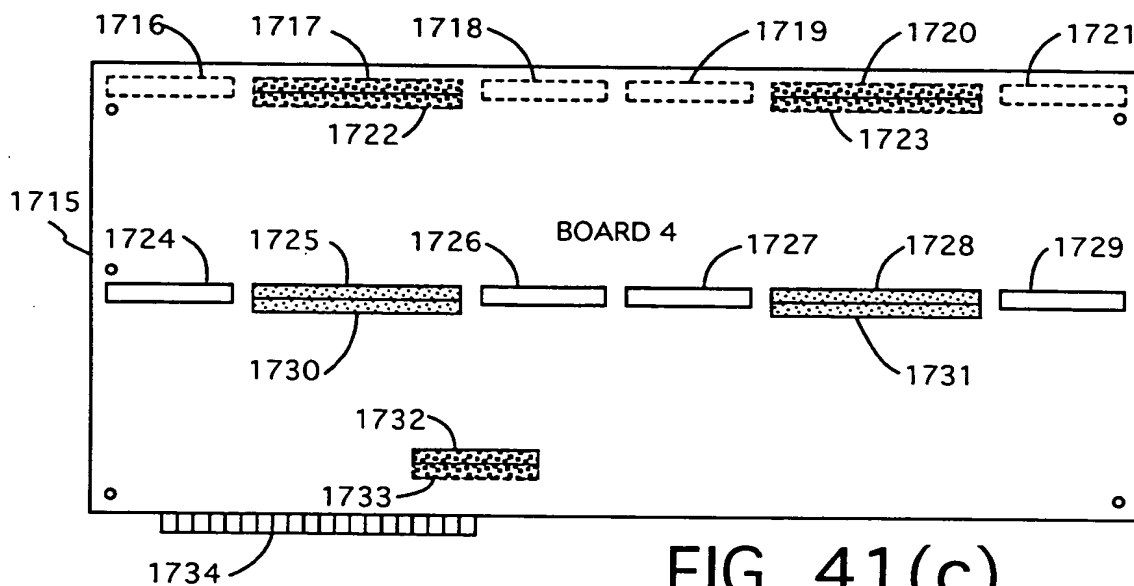


FIG. 40(b)





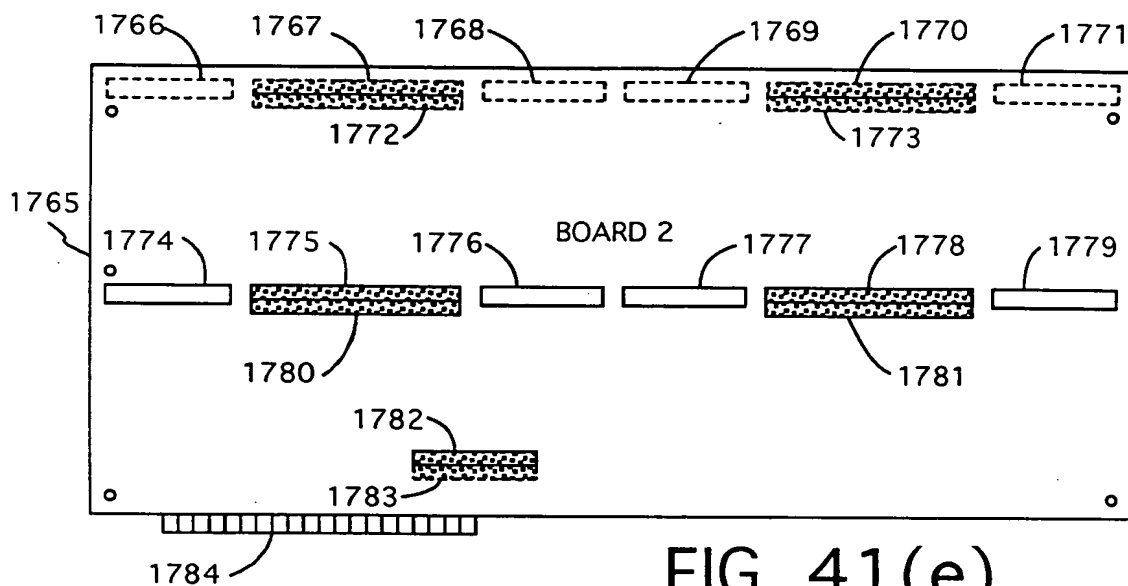


FIG. 41(e)

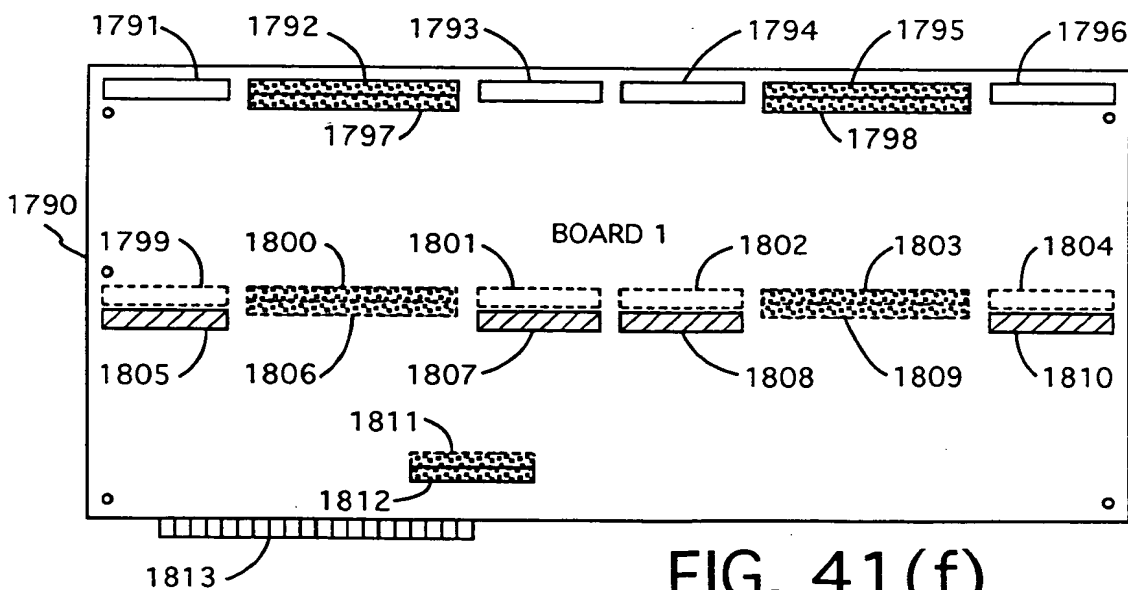
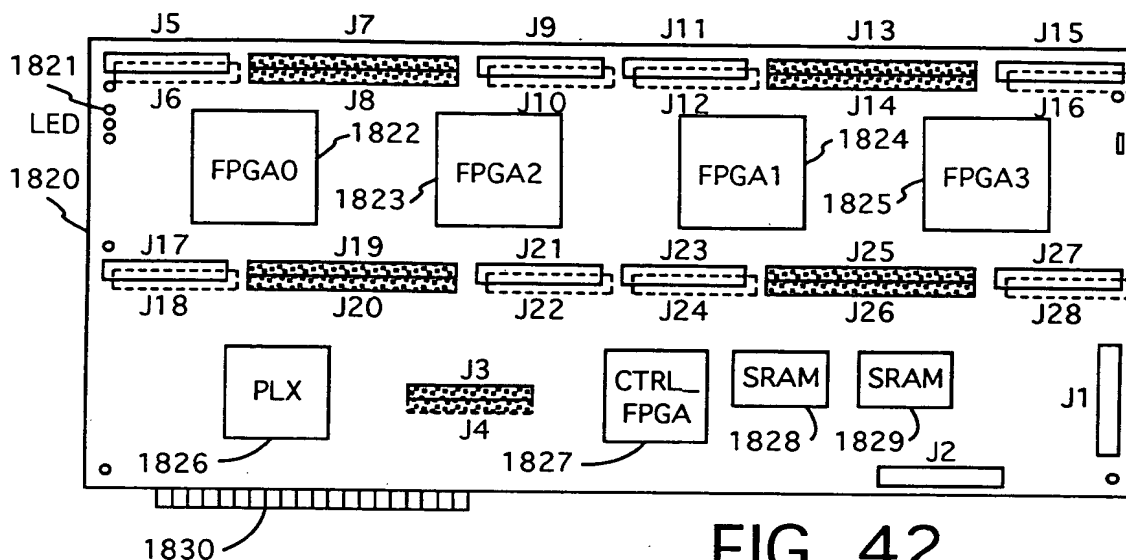






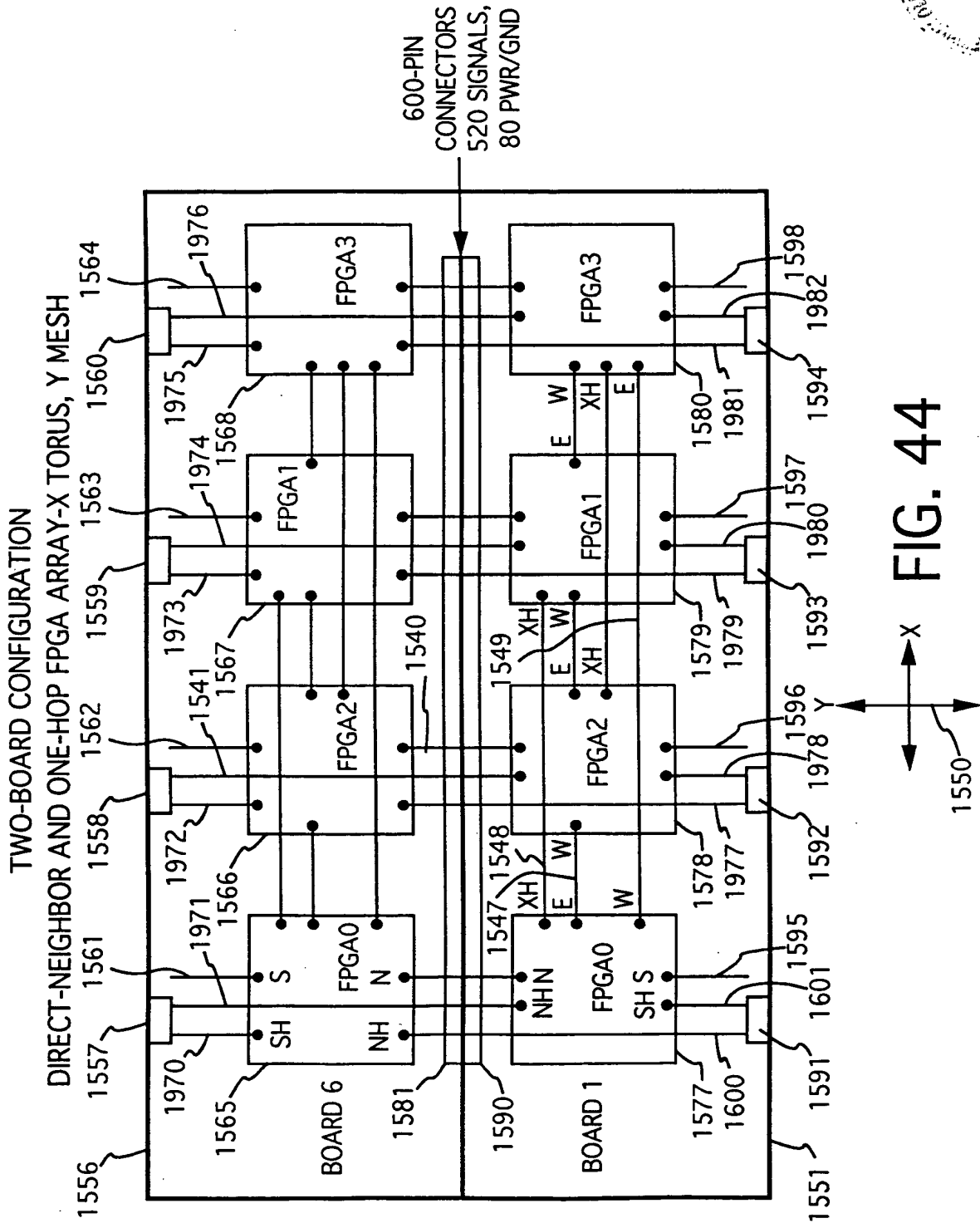


FIG. 41(f)



- | | | |
|------|---|---|
| 1840 |  | 2x30 HEADER, SMD, COMPONENT SIDE |
| 1841 |  | 2x30 RECEPTACLE, SMD, SOLDER SIDE |
| 1842 |  | 2x45, 2x30 HEADER, THRU HOLE, COMPONENT SIDE |
| 1843 |  | 2x45, 2x30 RECEPTACLE, THRU HOLE, SOLDER SIDE |
| 1844 |  | R-PACK, SMD, COMPONENT SIDE |
| 1845 |  | R-PACK, SMD, SOLDER SIDE |



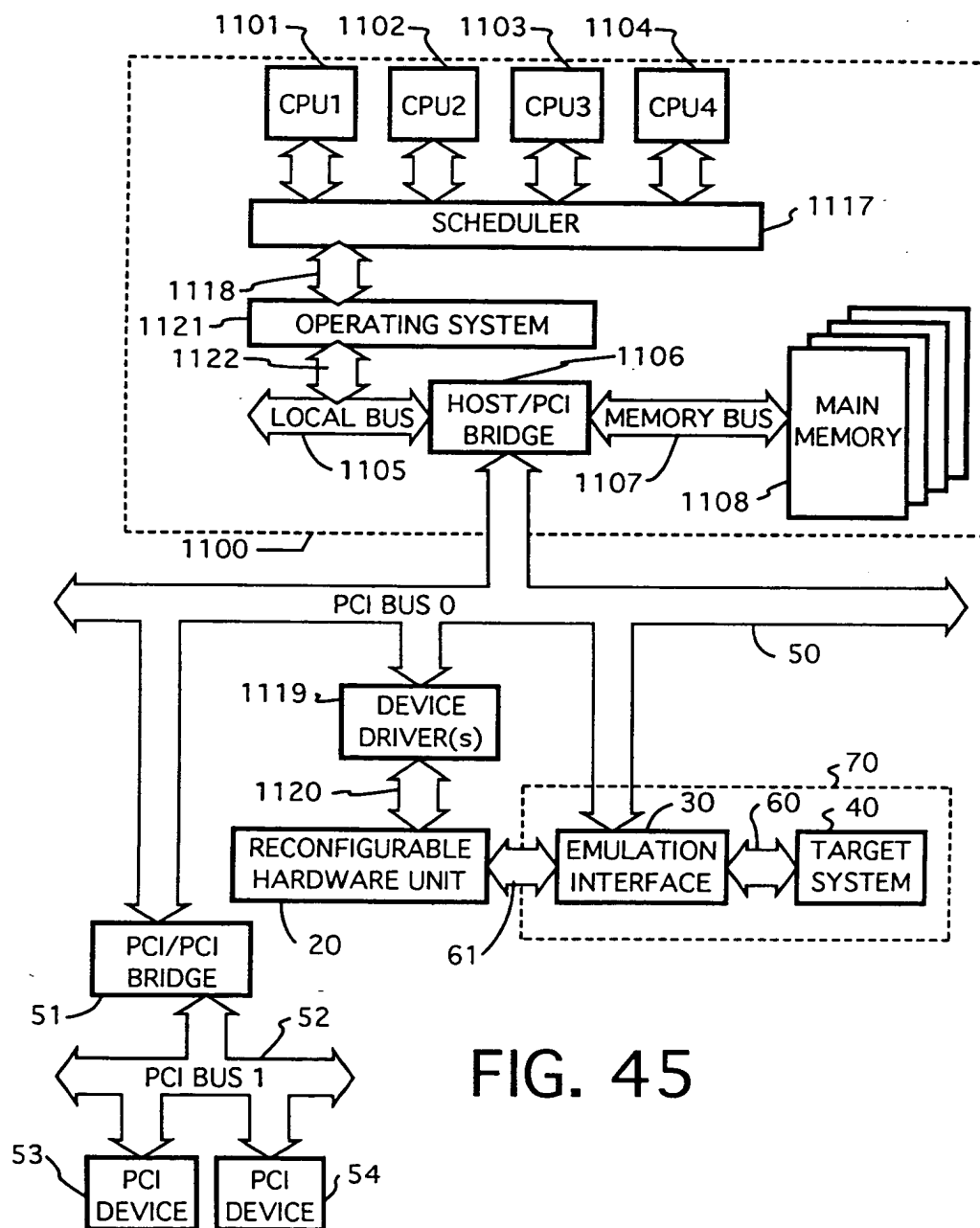


FIG. 45

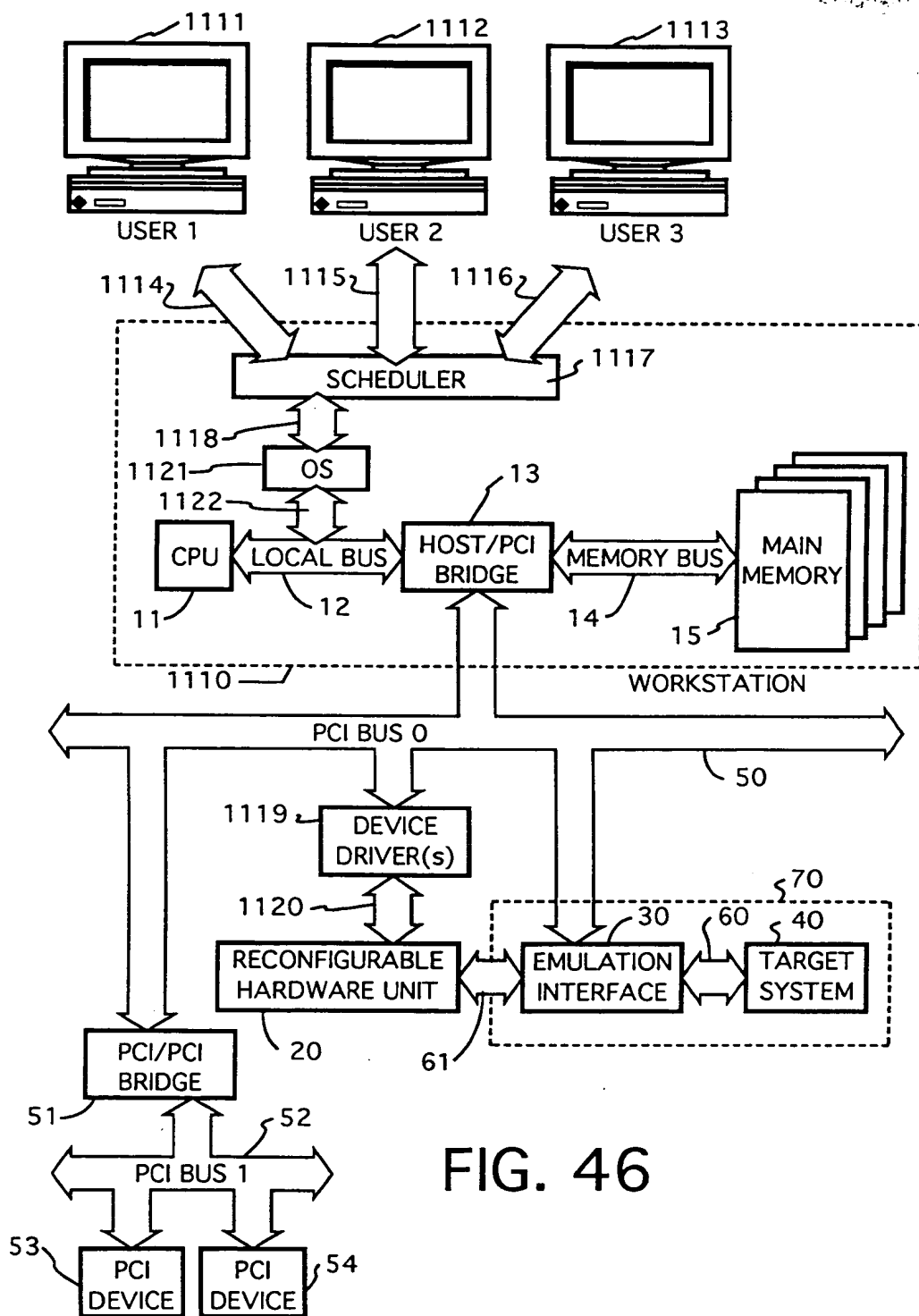


FIG. 46

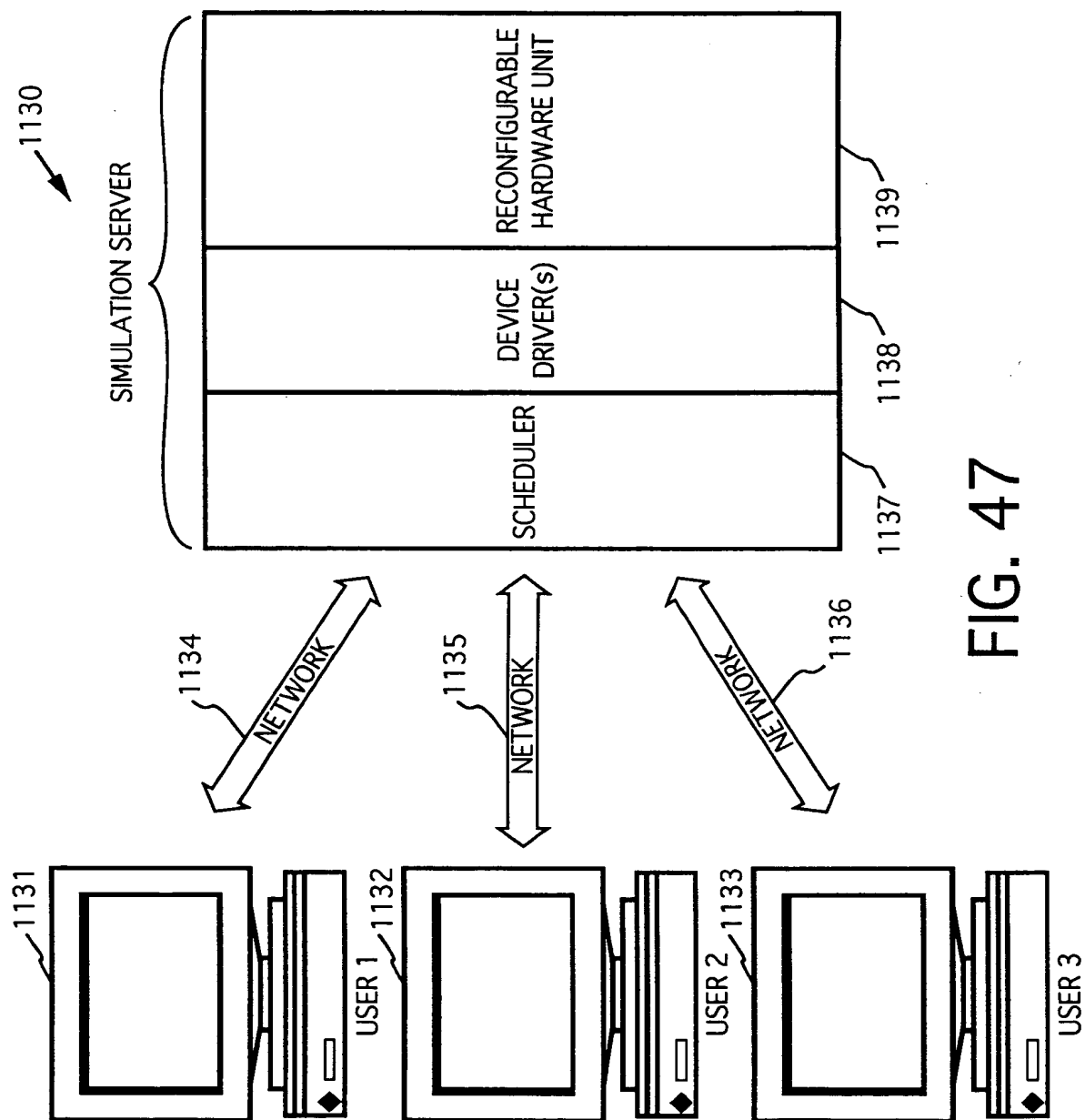


FIG. 47

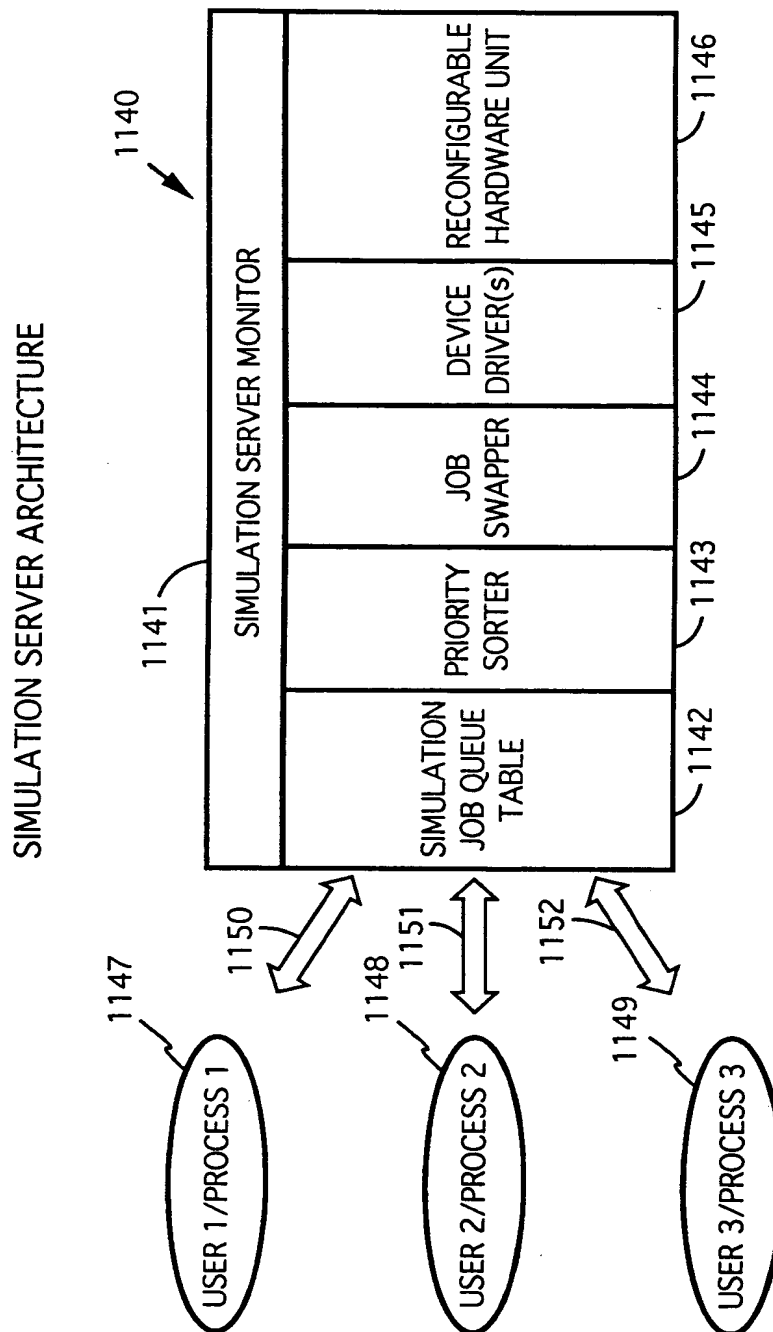


FIG. 48



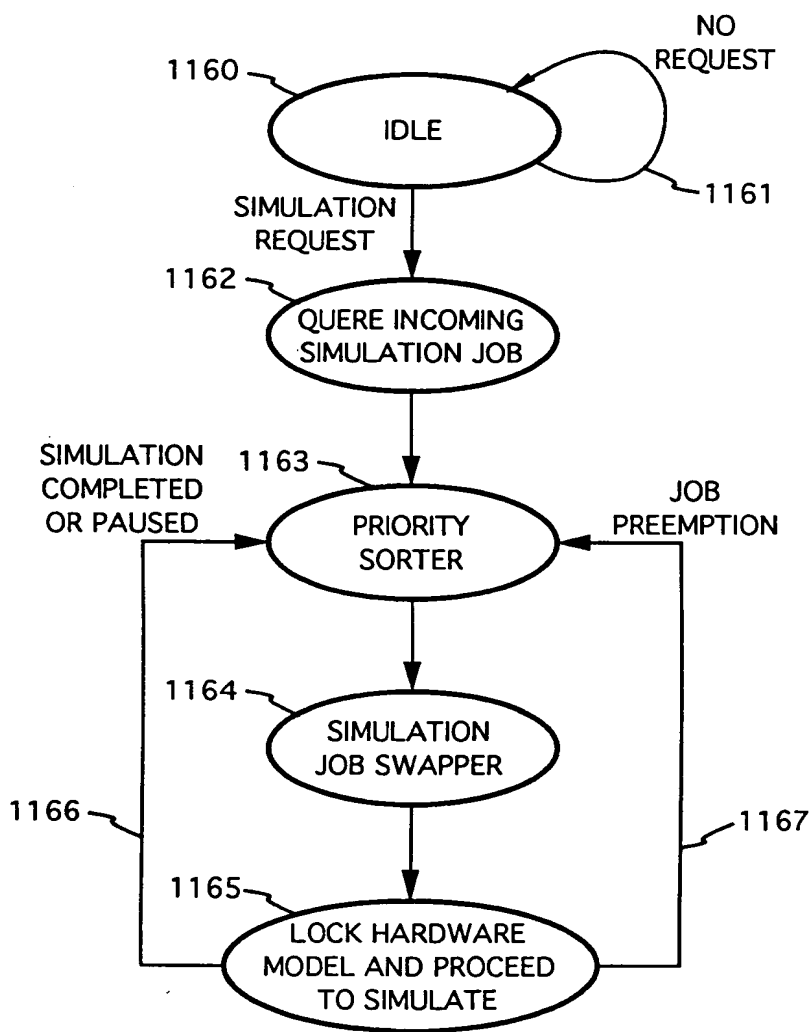


FIG. 49

JOB SWAPPER

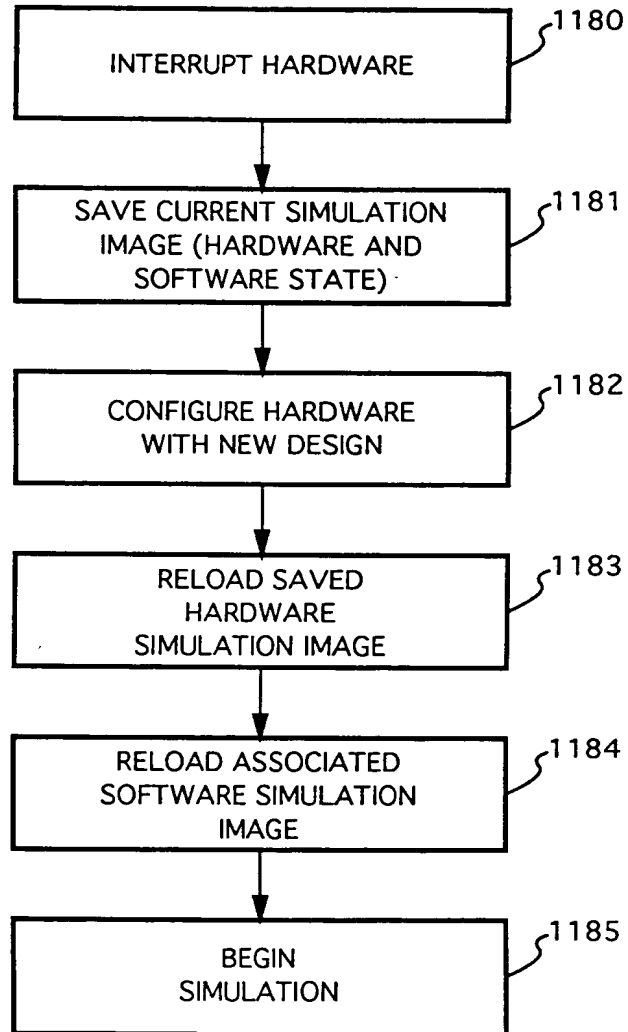


FIG. 50

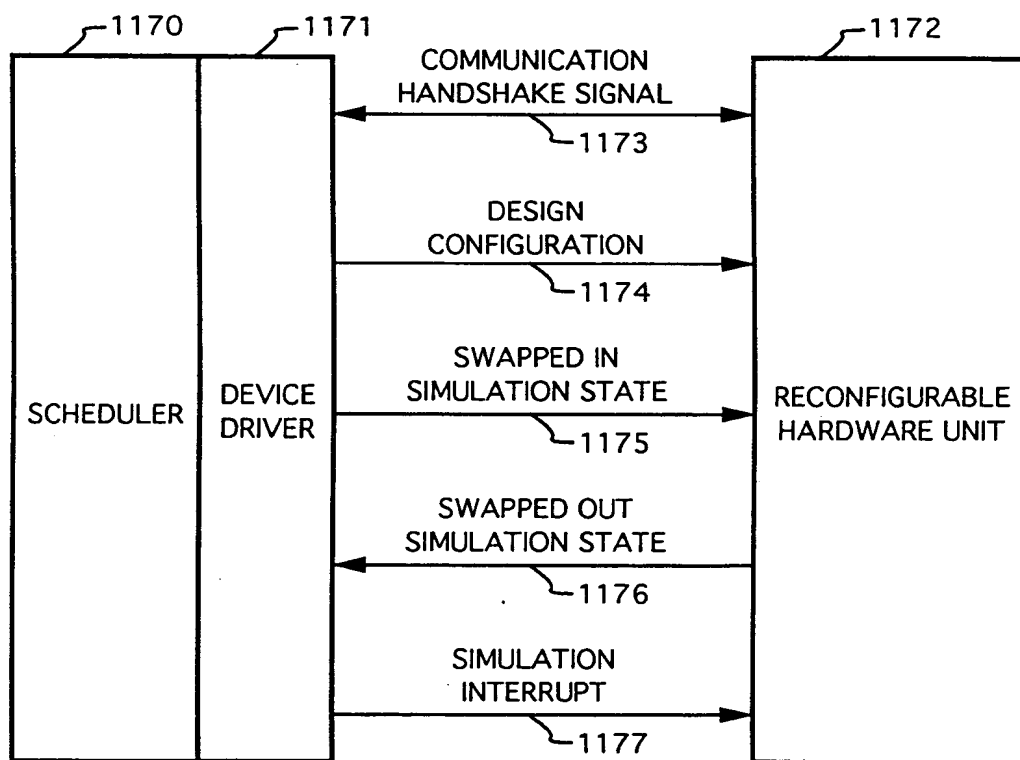


FIG. 51

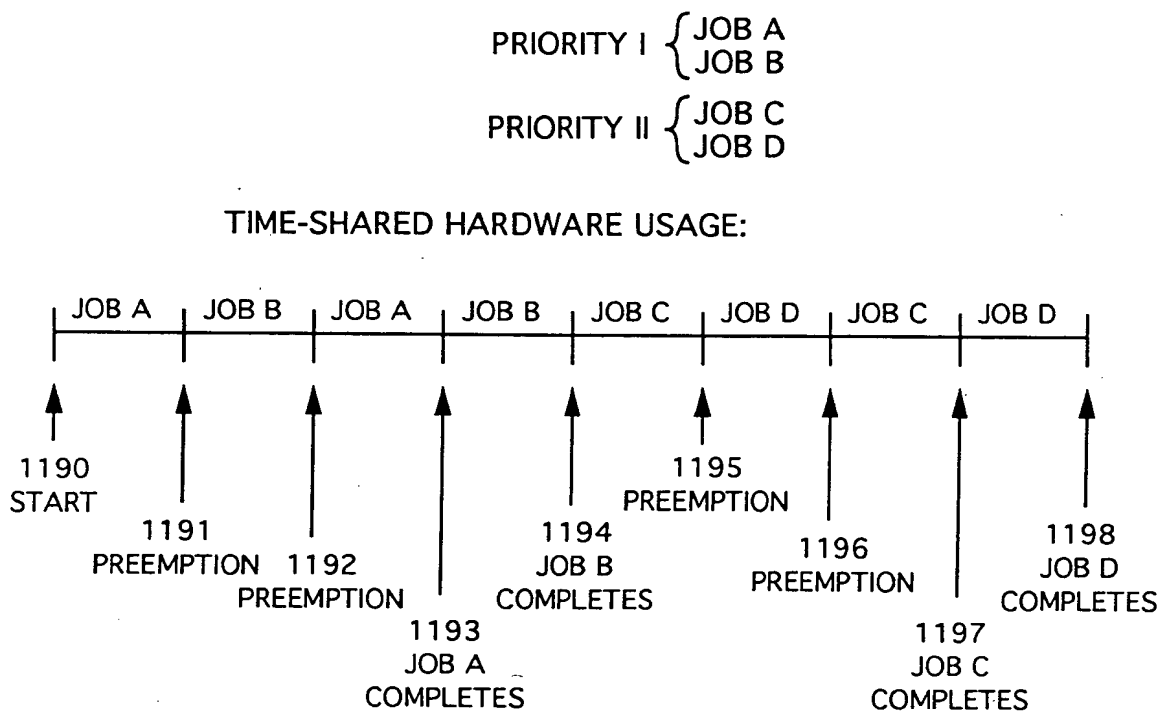


FIG. 52

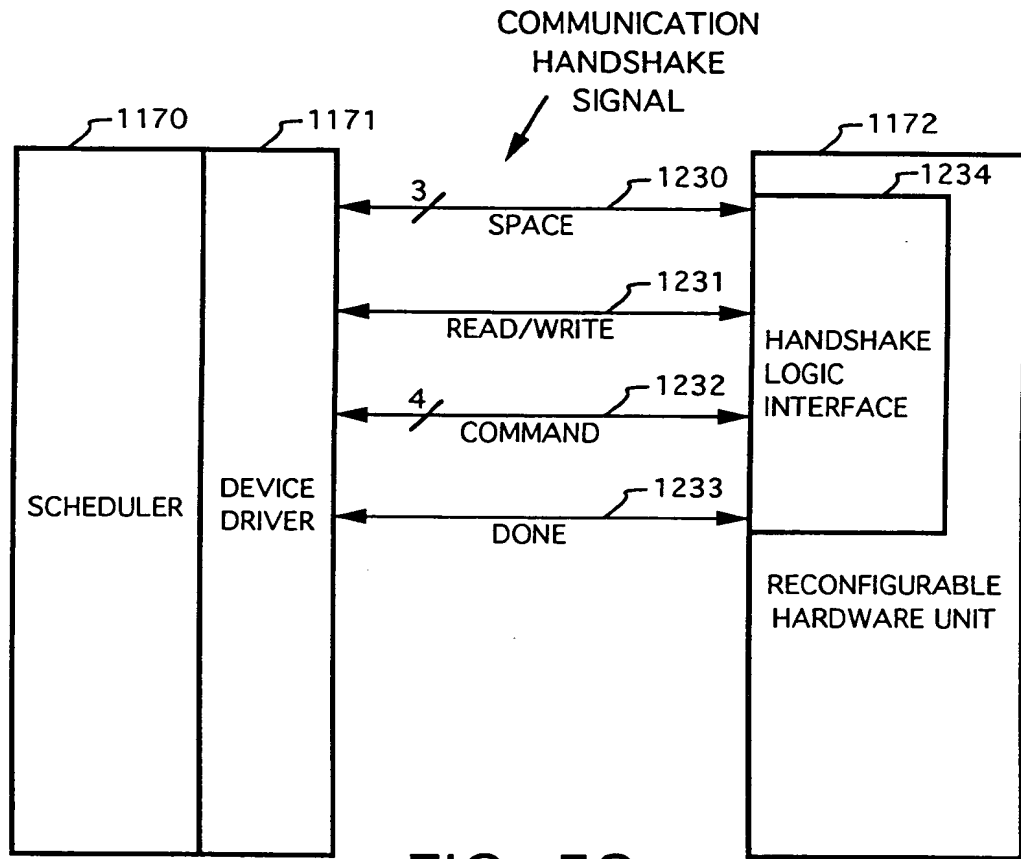


FIG. 53

FIG. 54

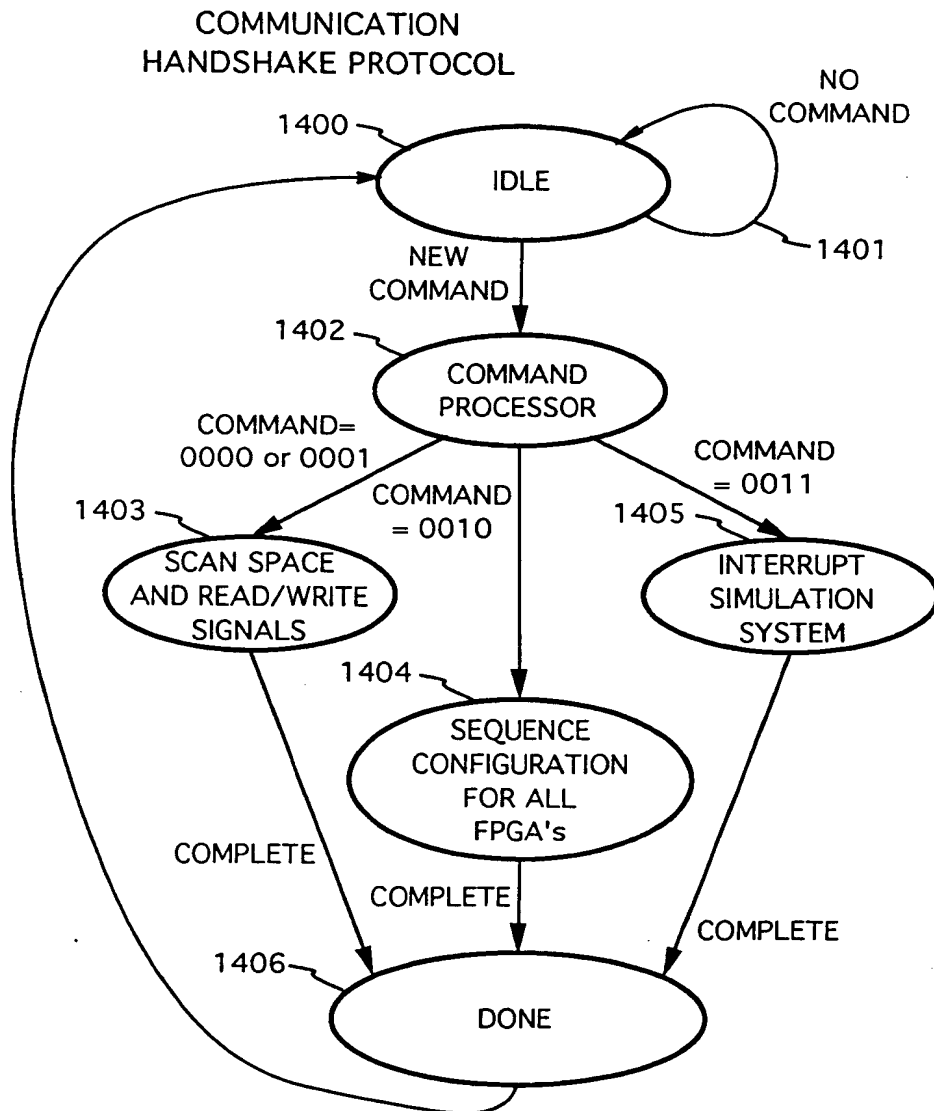


FIG. 54

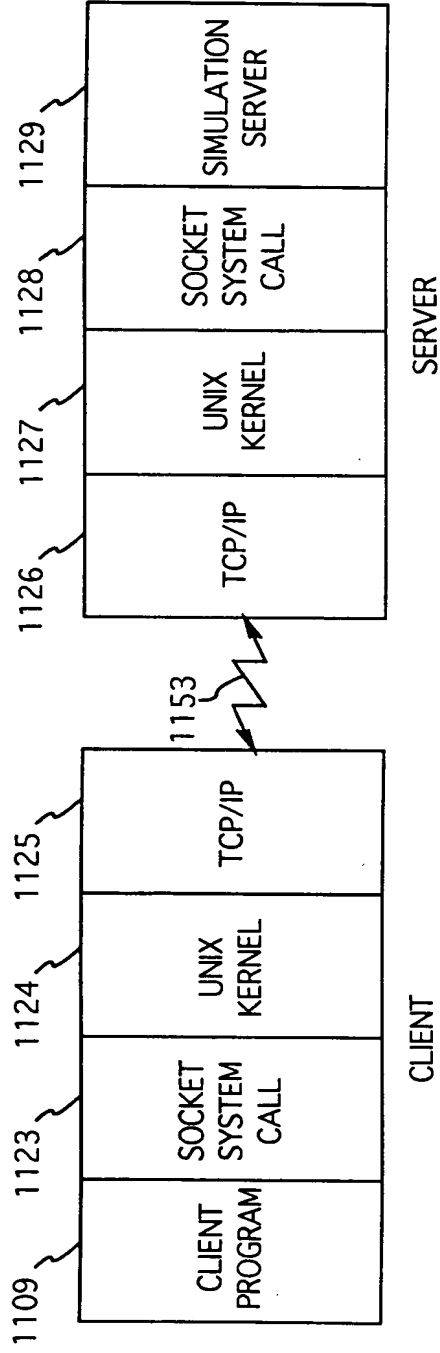
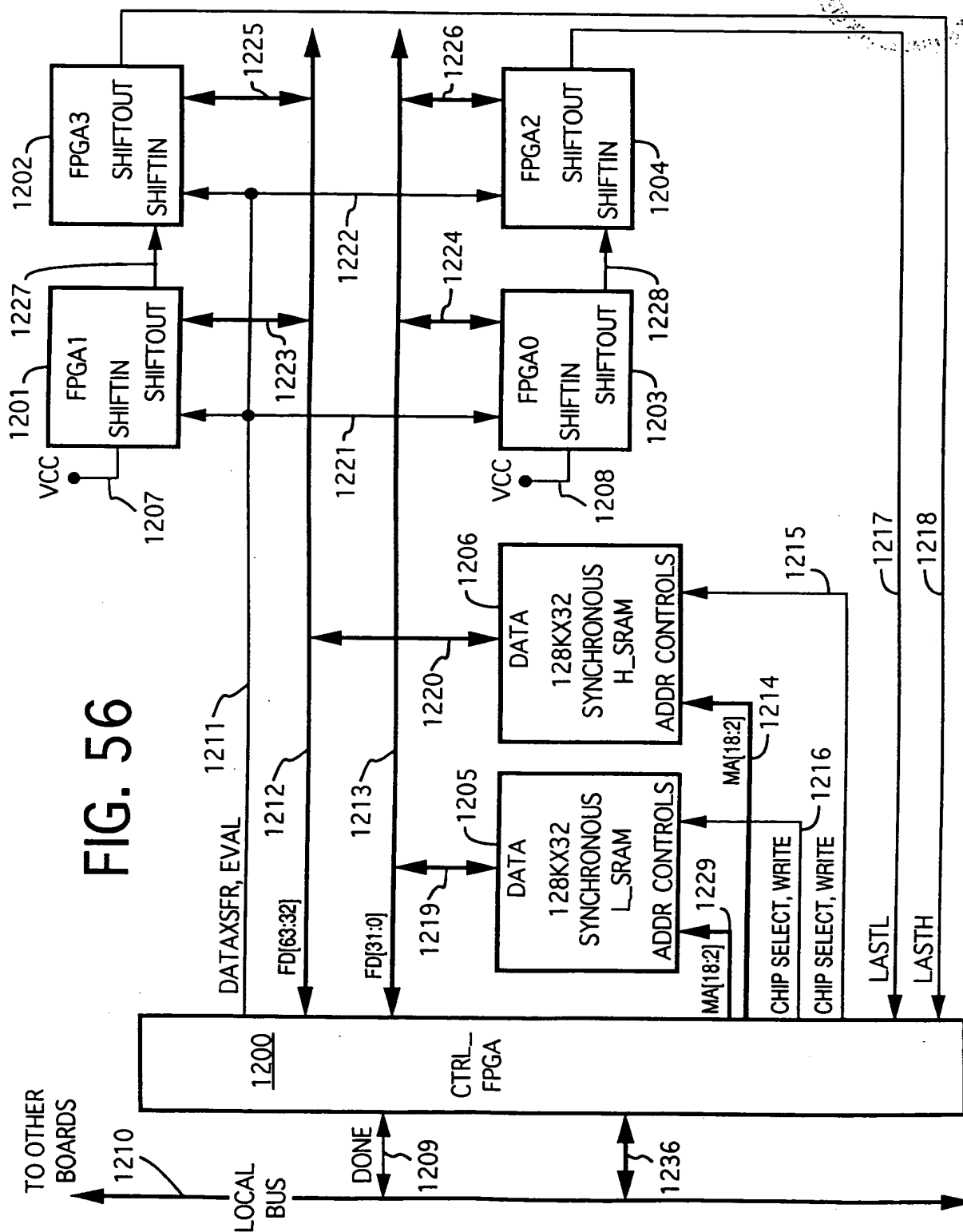
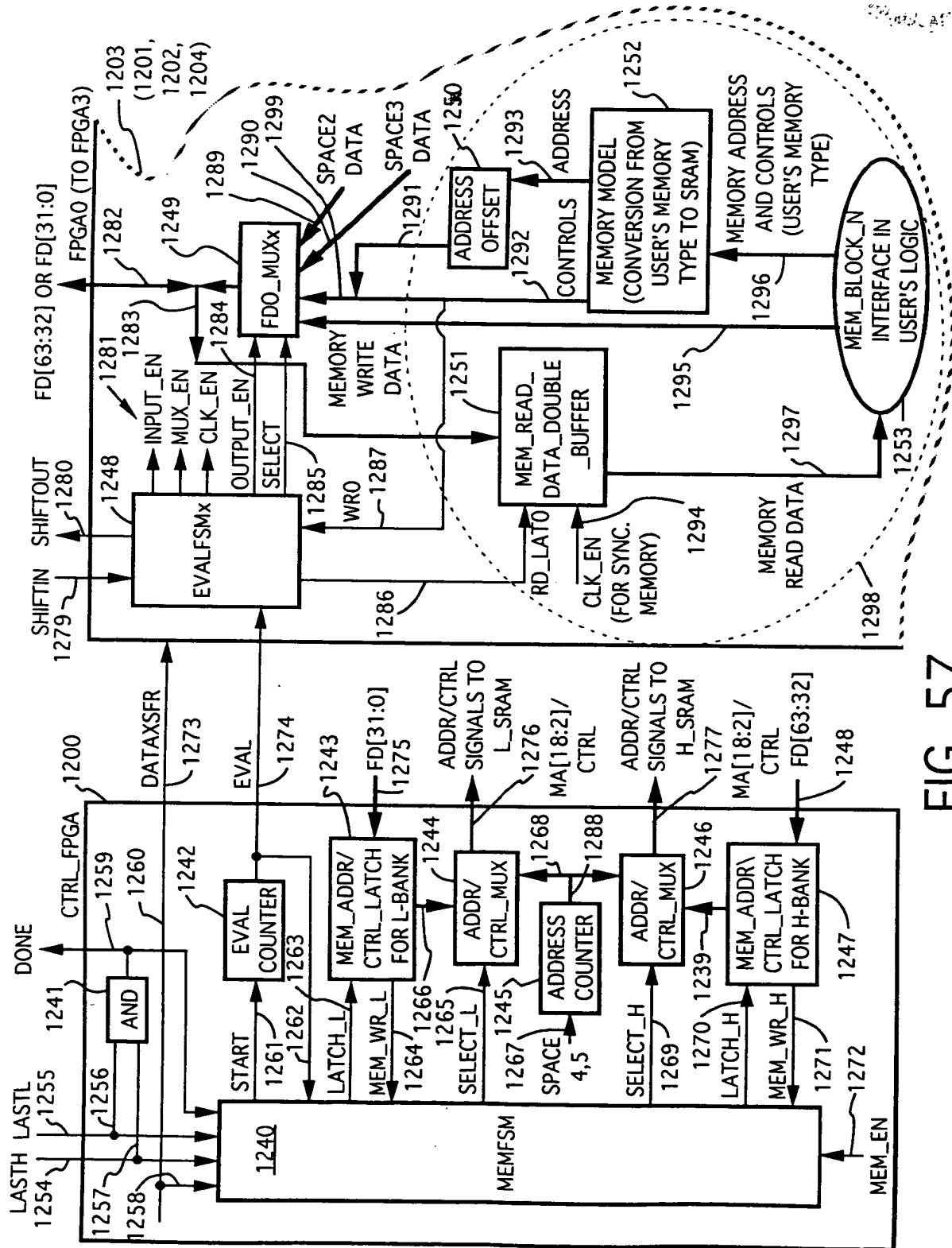


FIG. 55





0900124-101001

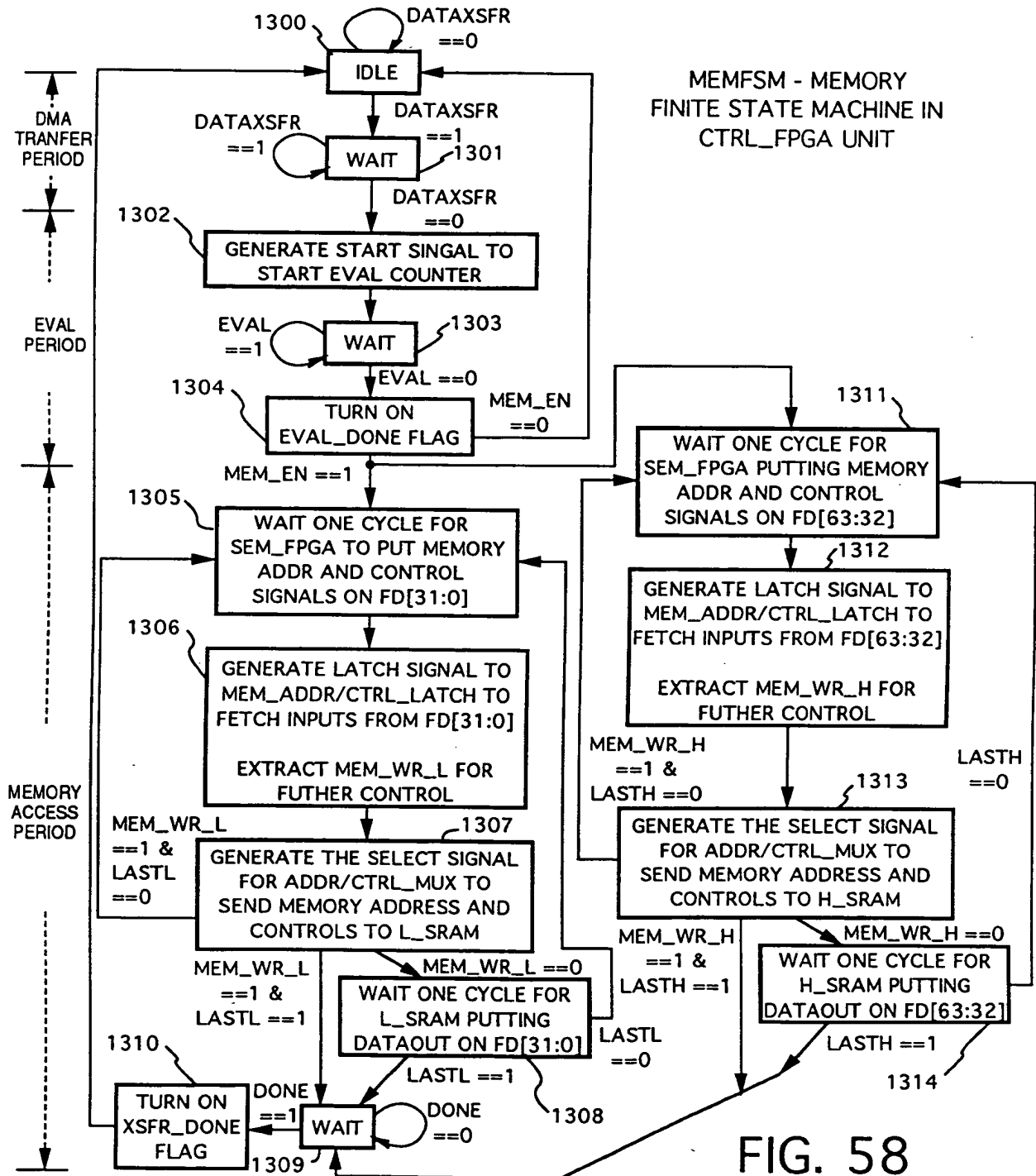


FIG. 58

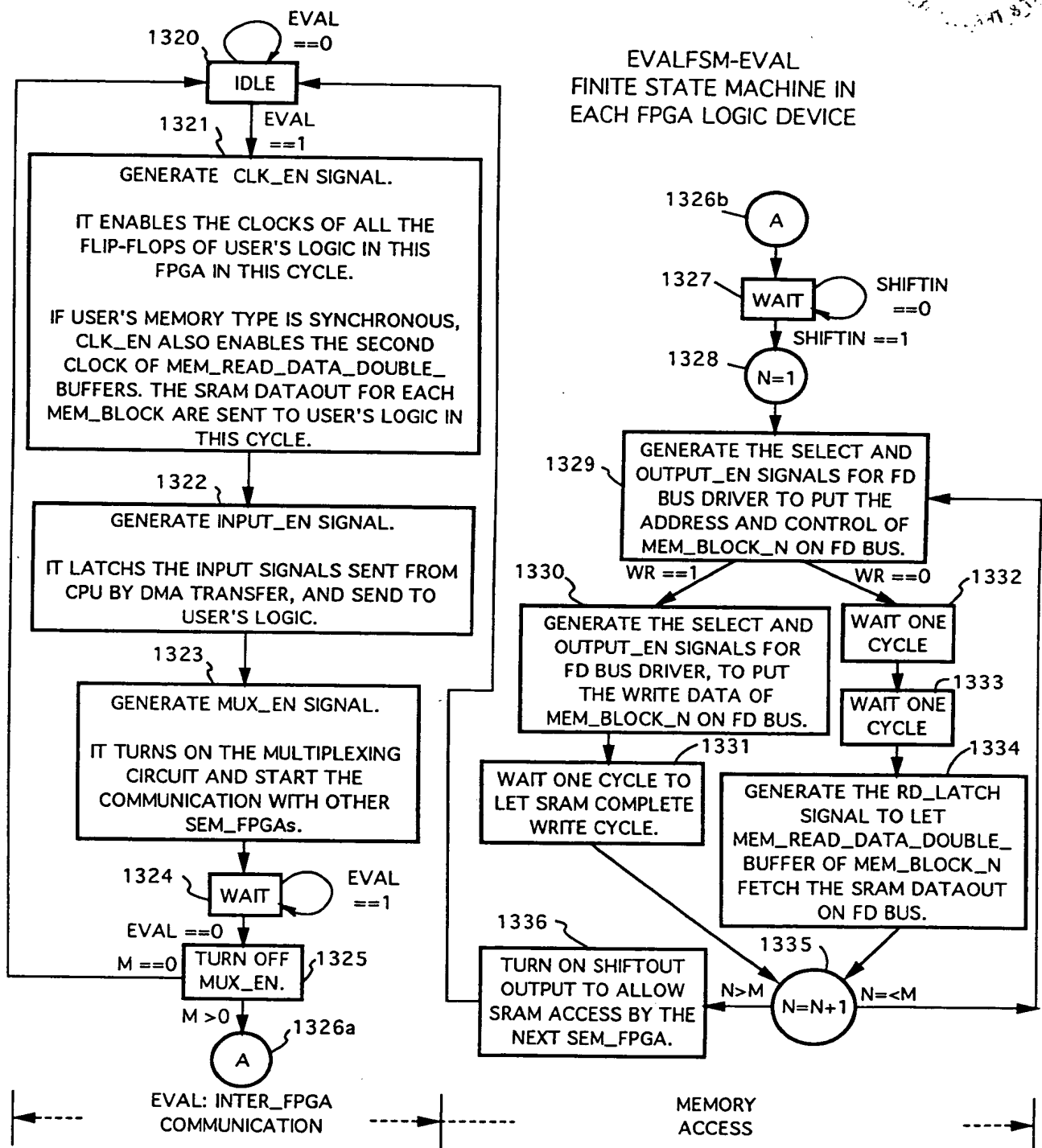


FIG. 59

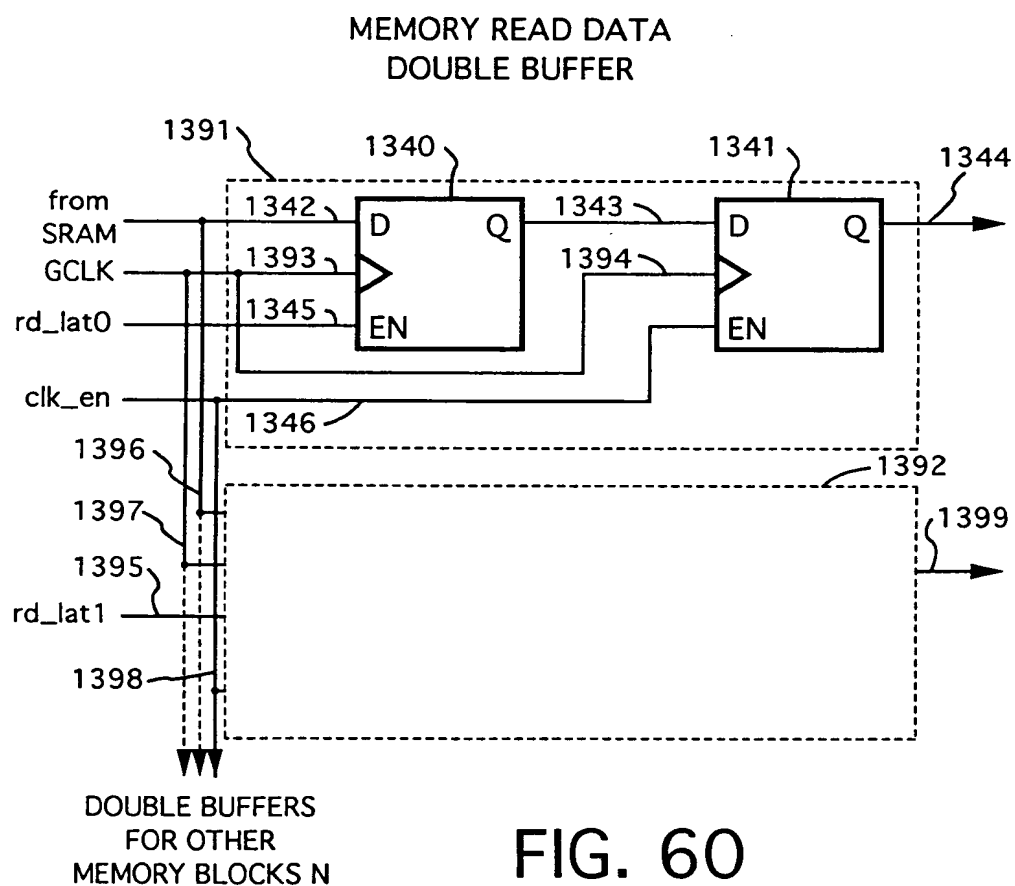
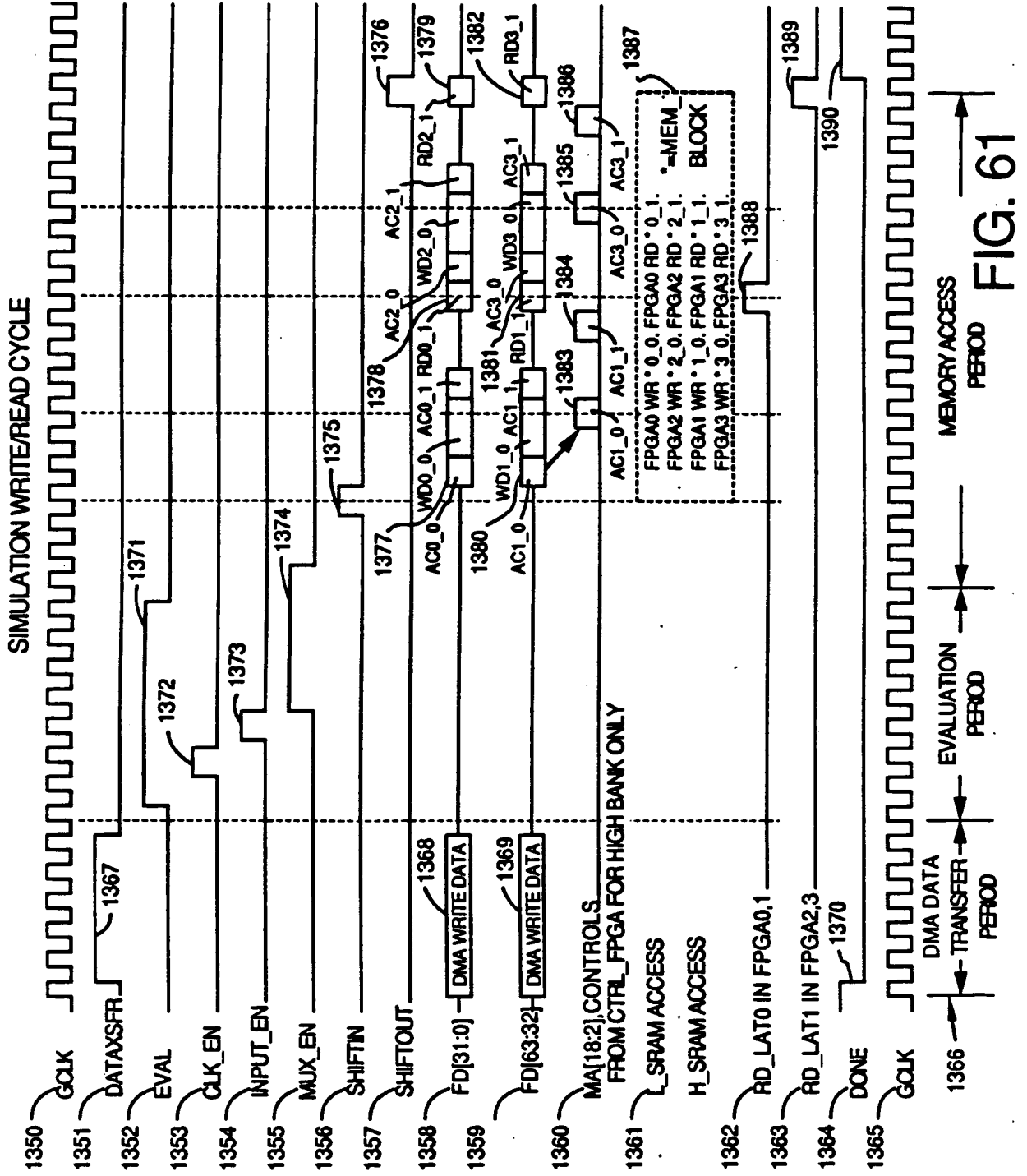


FIG. 60

09900124-101001



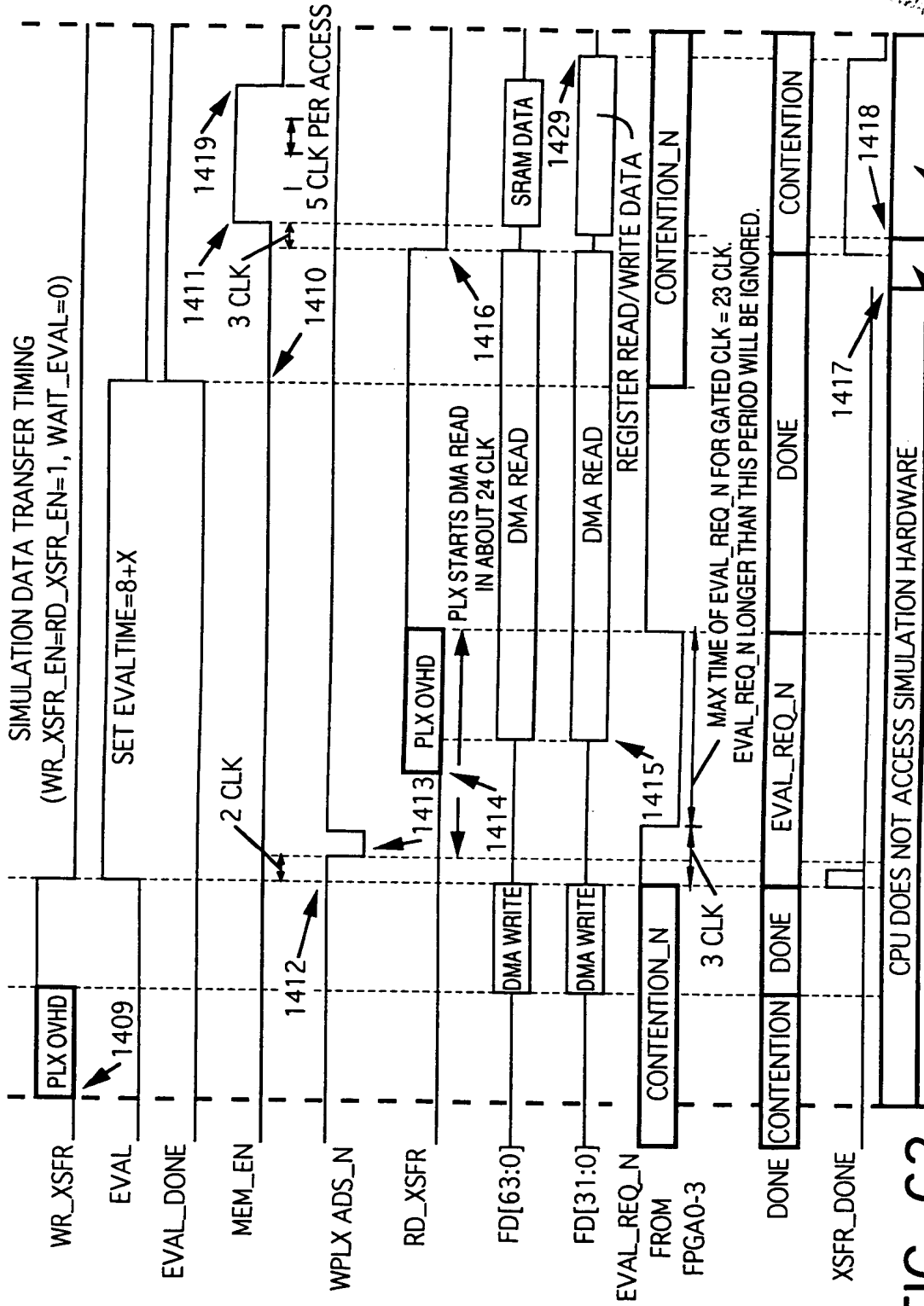


FIG. 62

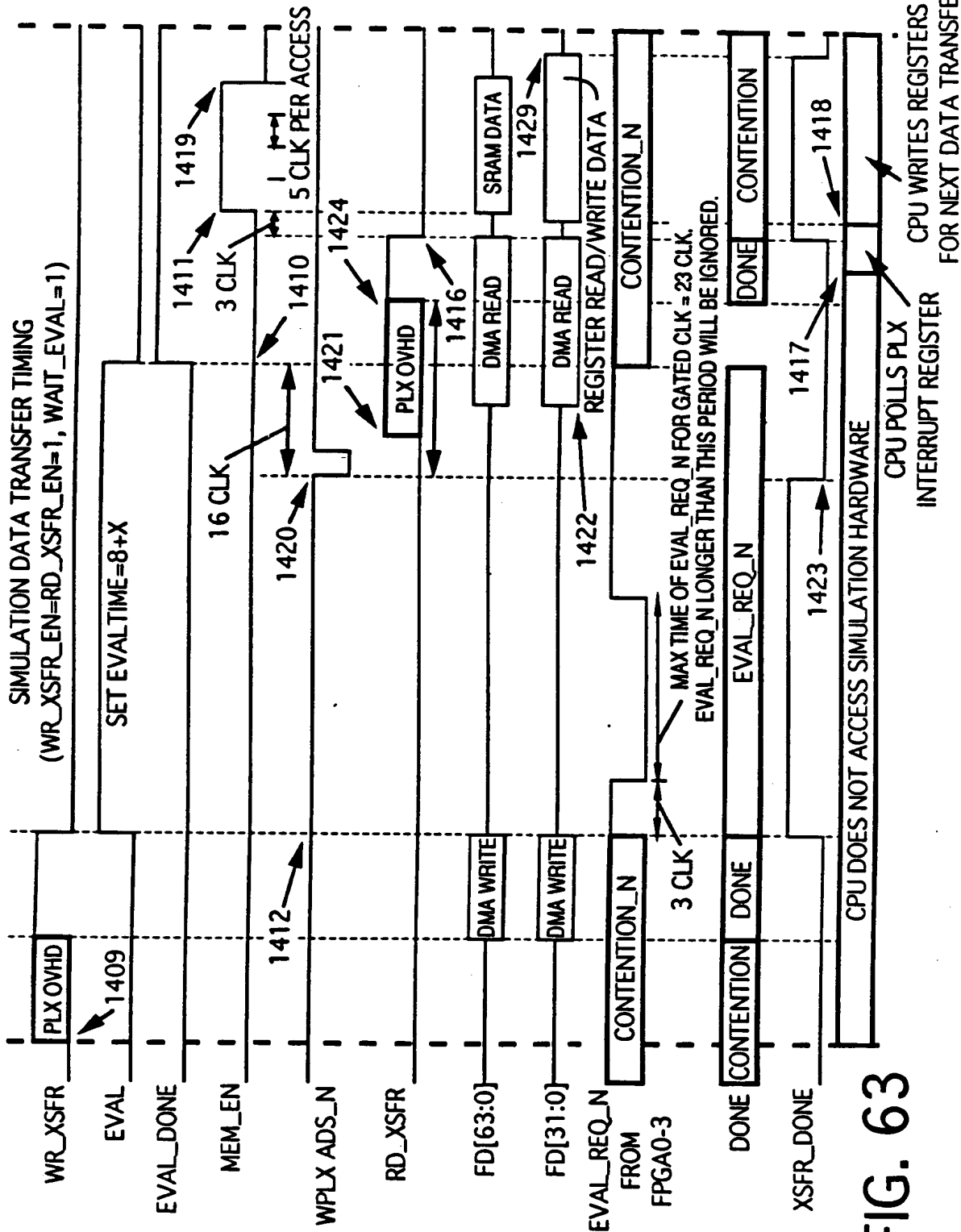


FIG. 63

Typical User Design of PCI Add-on Cards

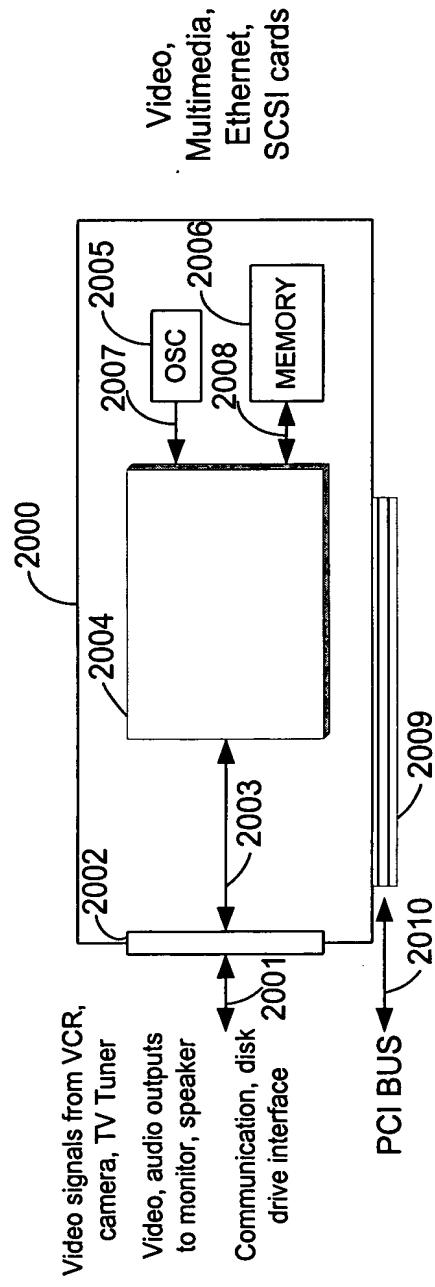
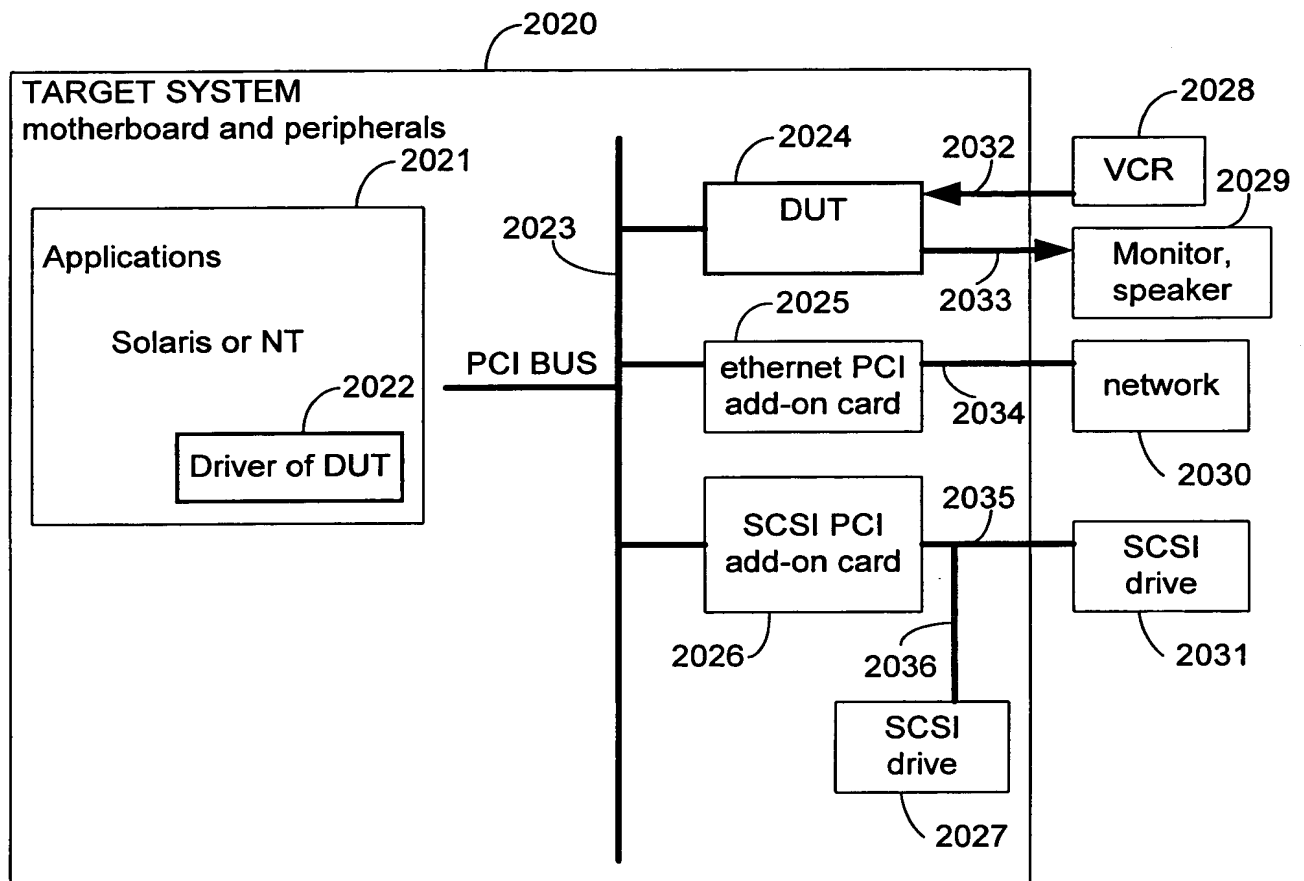


FIG. 64



Typical Hardware/Software Co-Verification

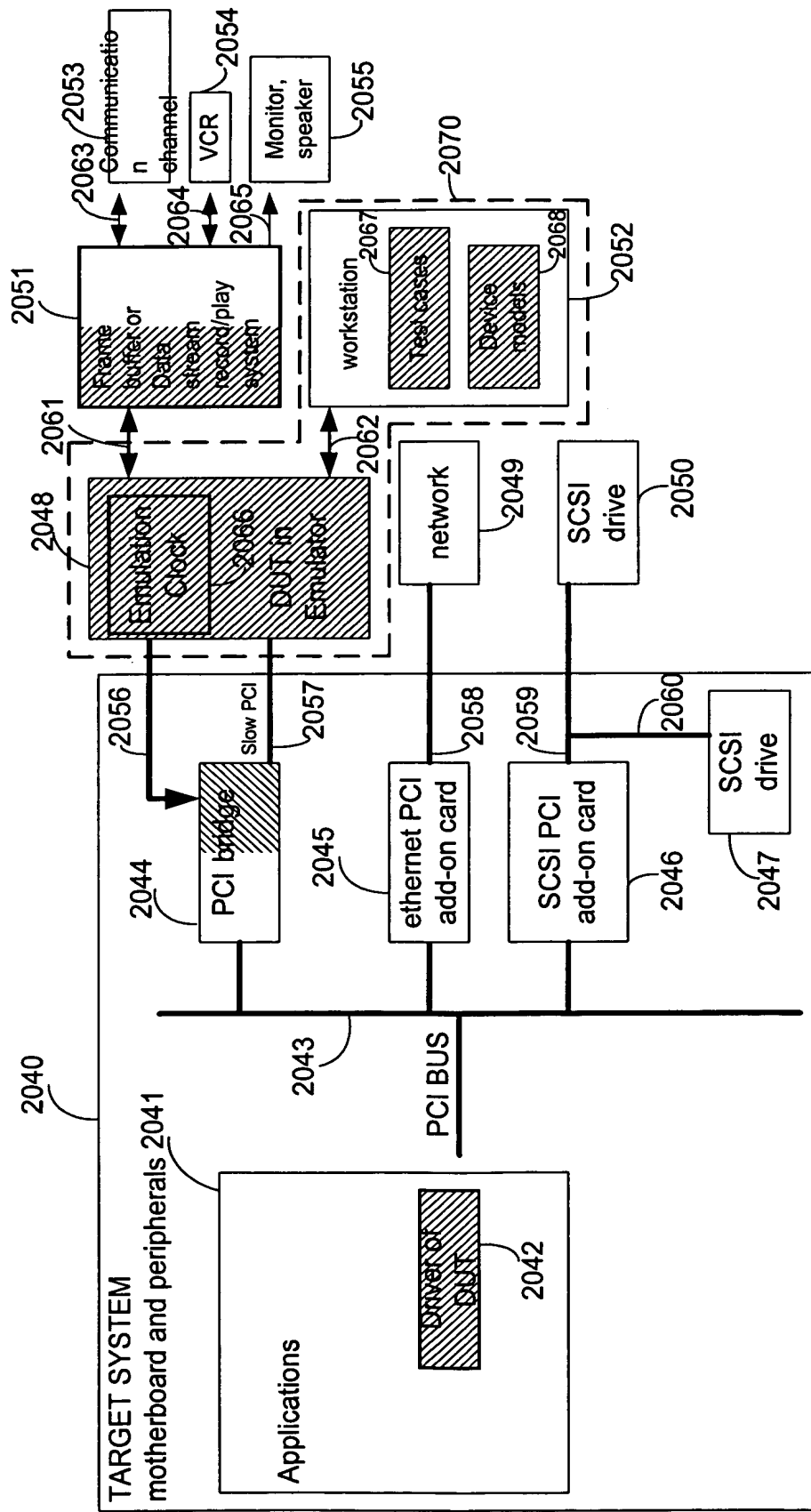


 : DUT (Device Under Test)

FIG. 65

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Typical Co-Verification by Using Emulator



: running time at emulation speed

The rest of the target system is running at full speed.

FIG. 66

SIMULATION

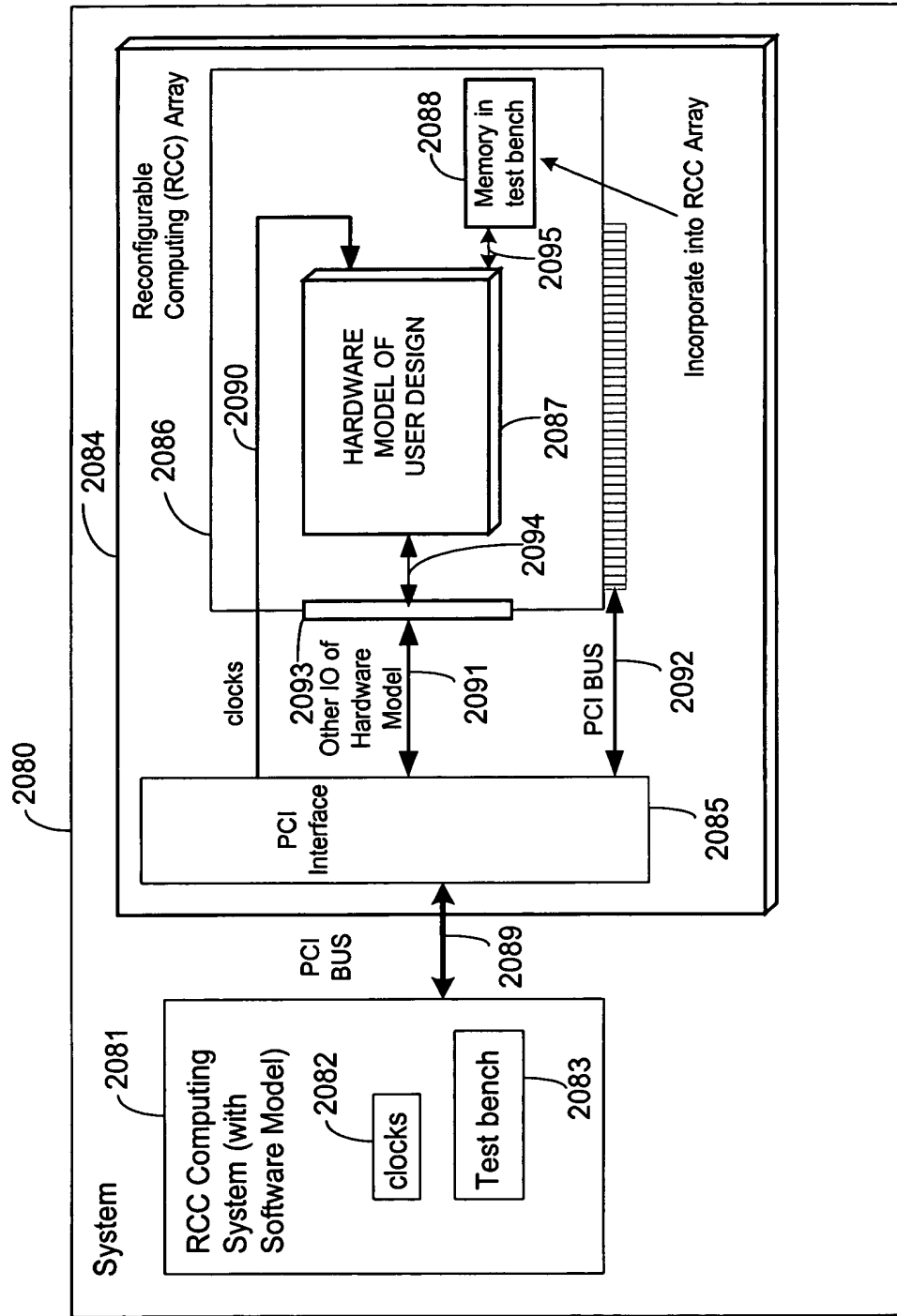


FIG. 67

CO-VERIFICATION WITHOUT EXTERNAL I/O

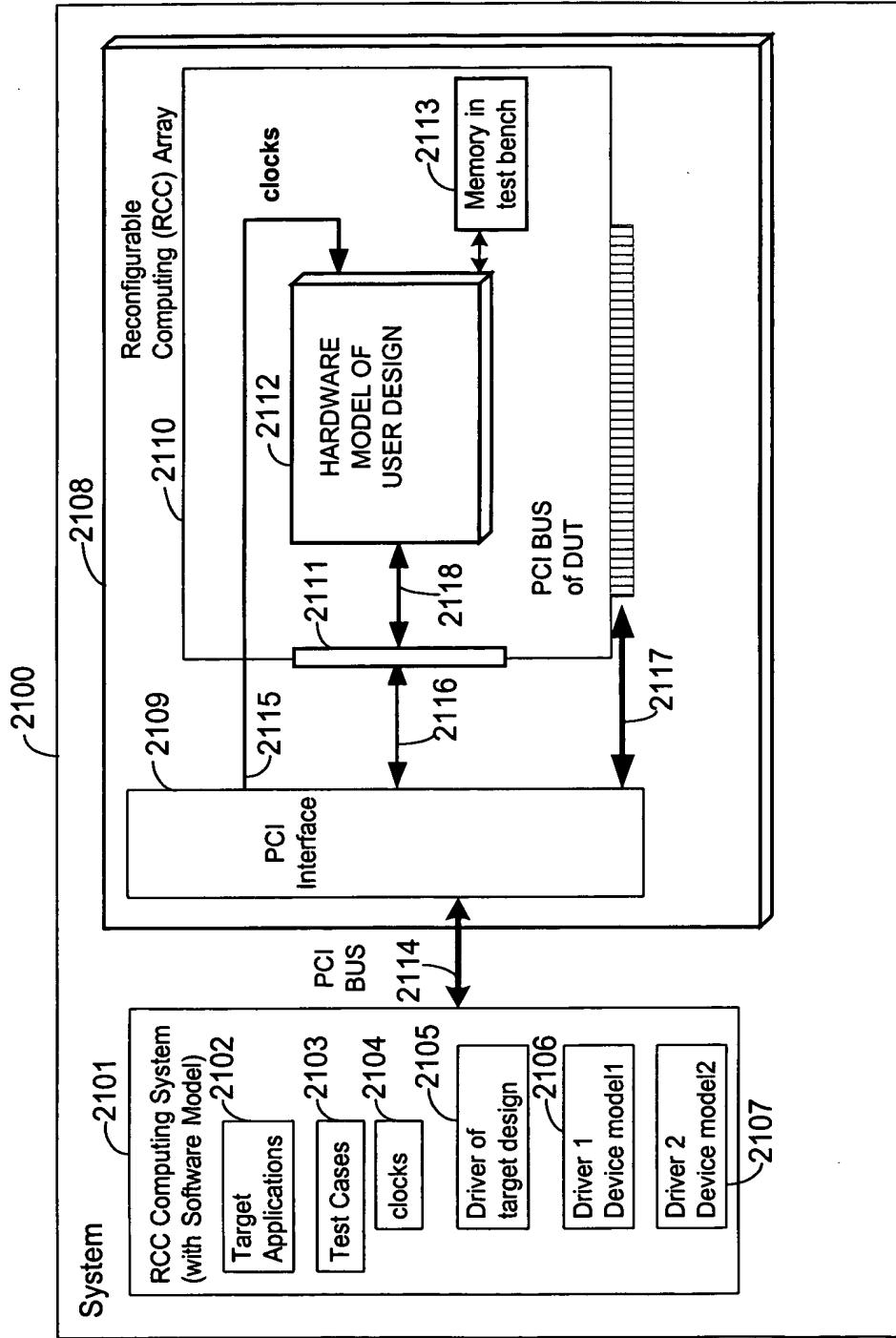


FIG. 68

CO-VERIFICATION WITH EXTERNAL I/O

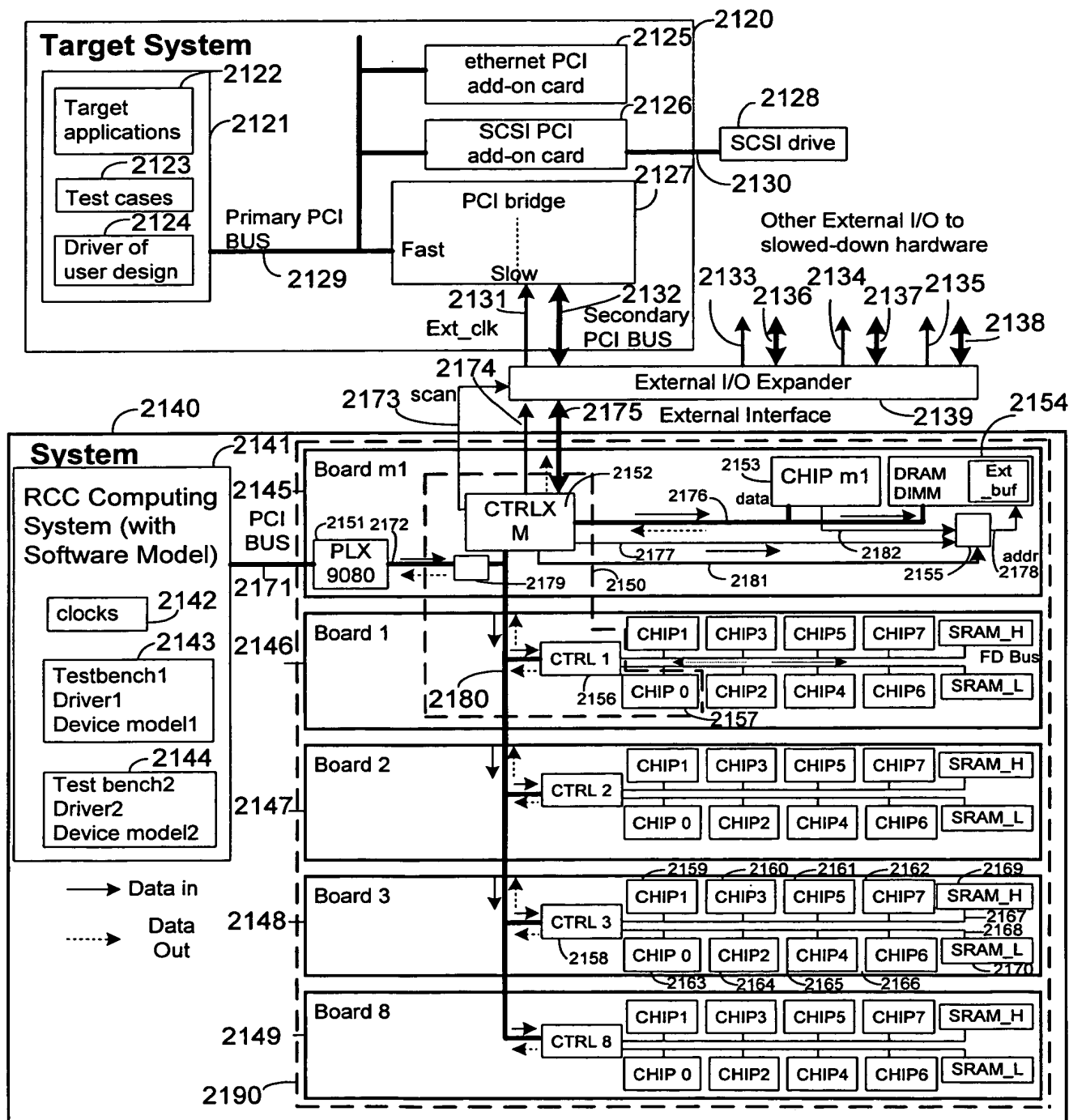


FIG. 69

CONTROL OF DATA-IN CYCLE

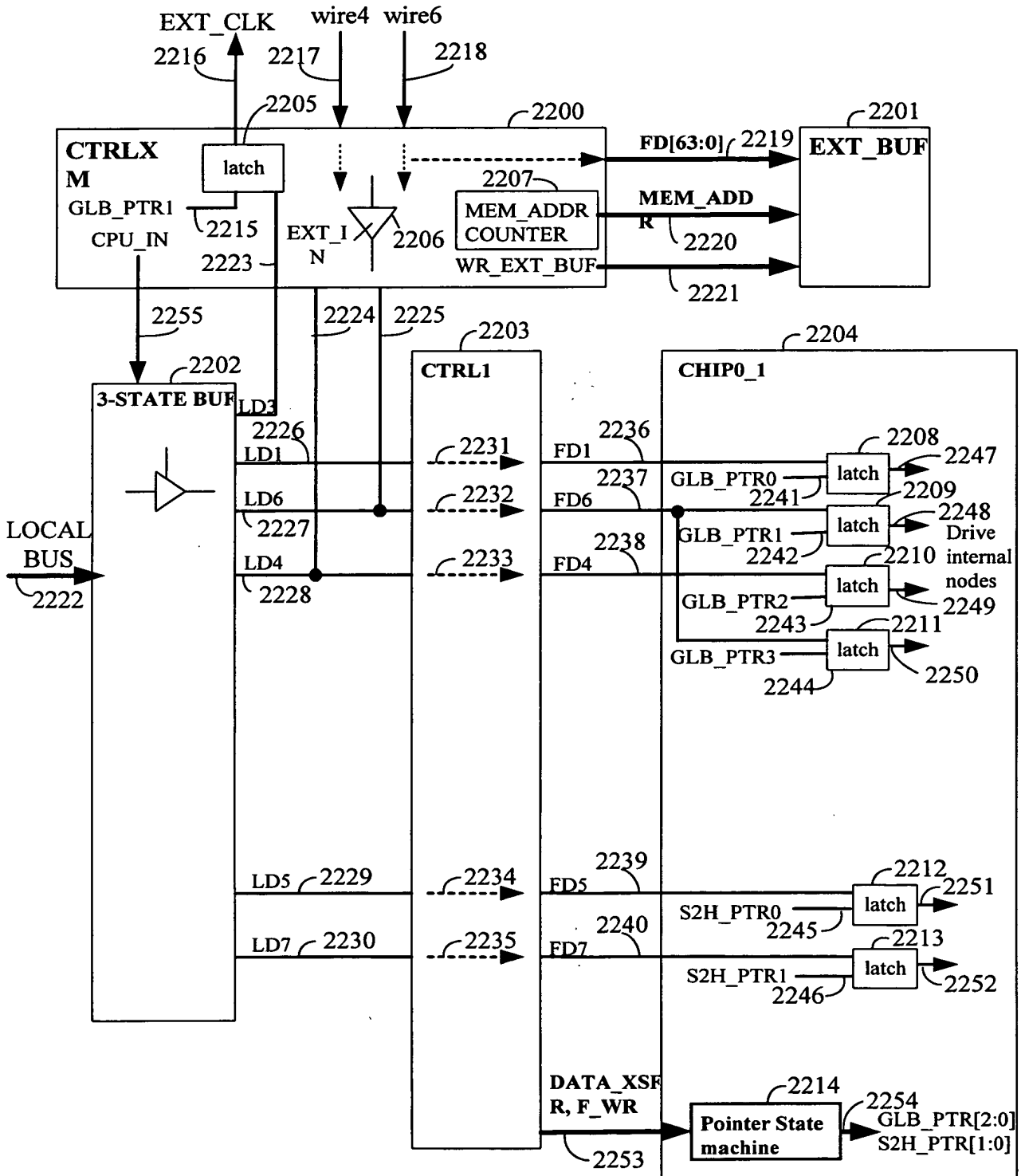


FIG. 70

FIG. 70

CONTROL OF DATA-OUT CYCLE

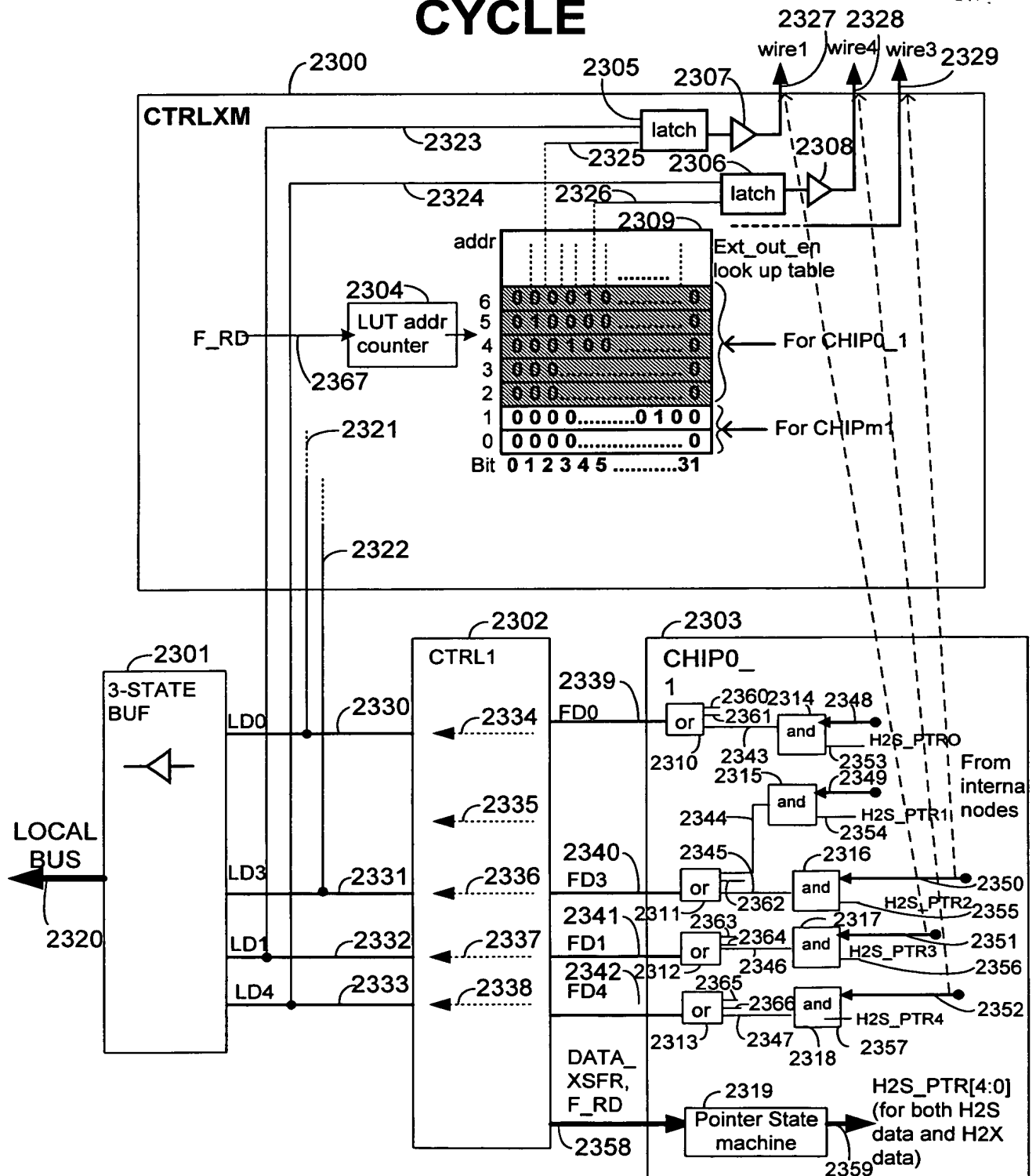


FIG. 71

CONTROL OF DATA-IN CYCLE

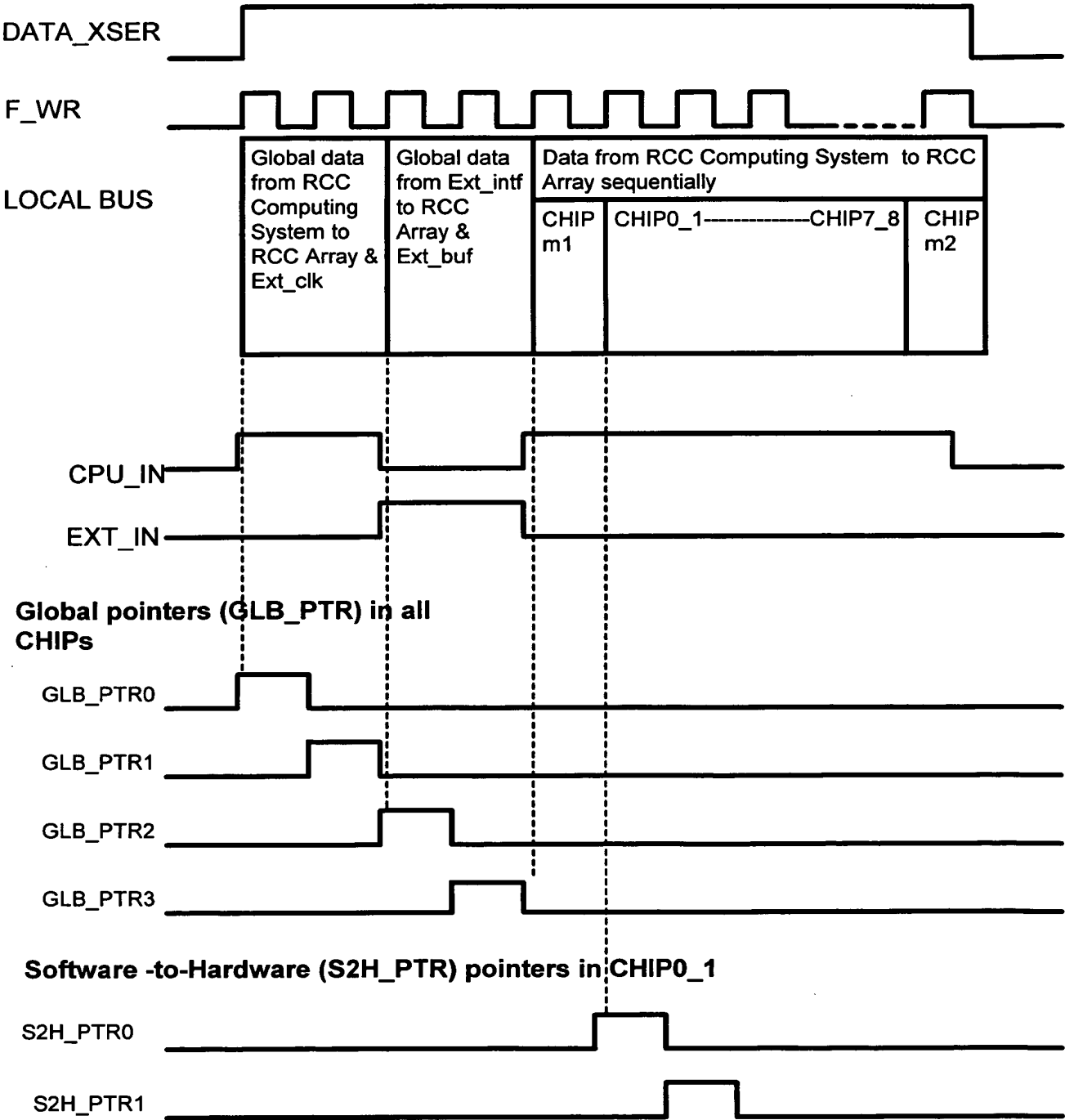


FIG. 72

CONTROL OF DATA-OUT CYCLE

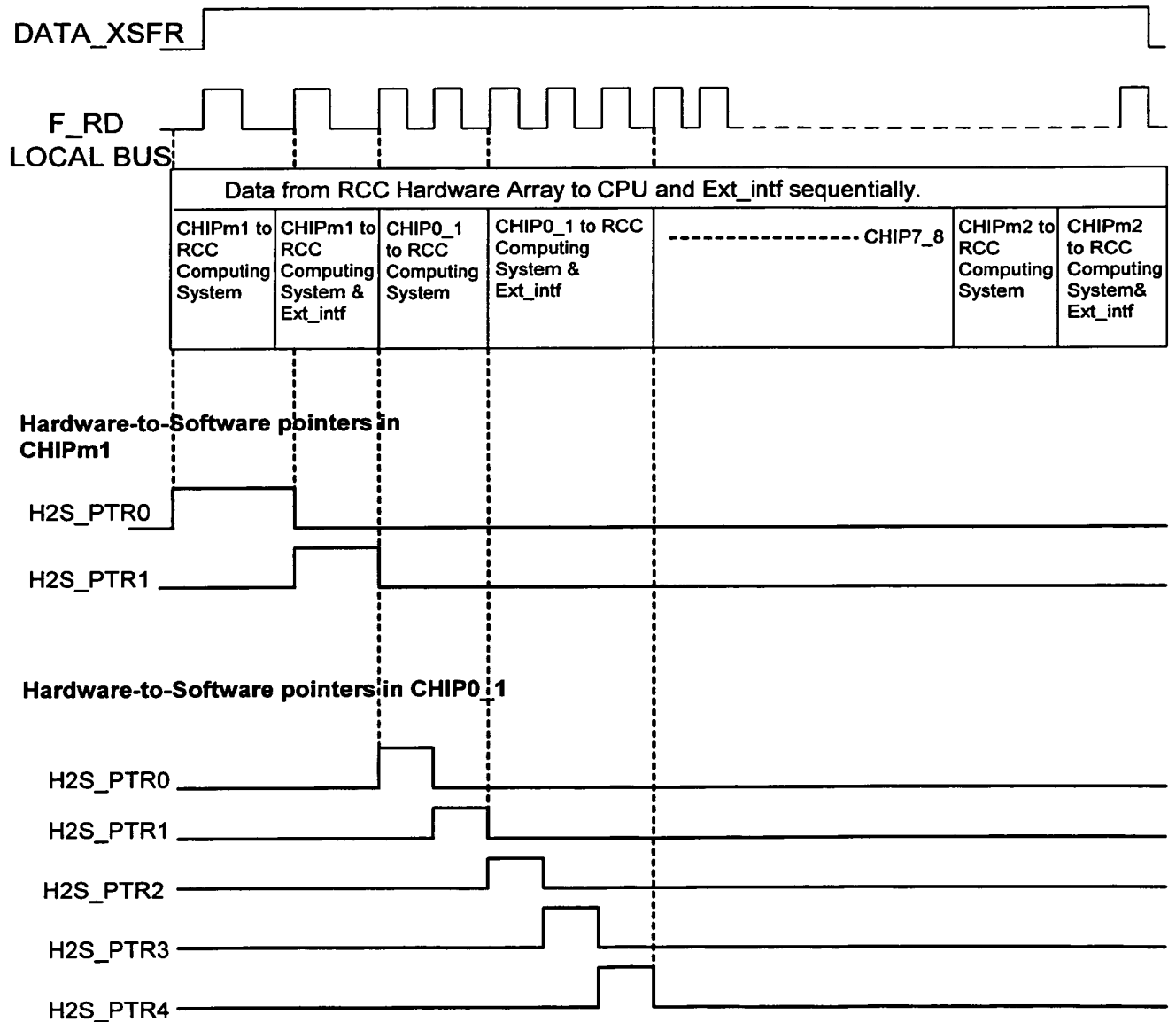


FIG. 73

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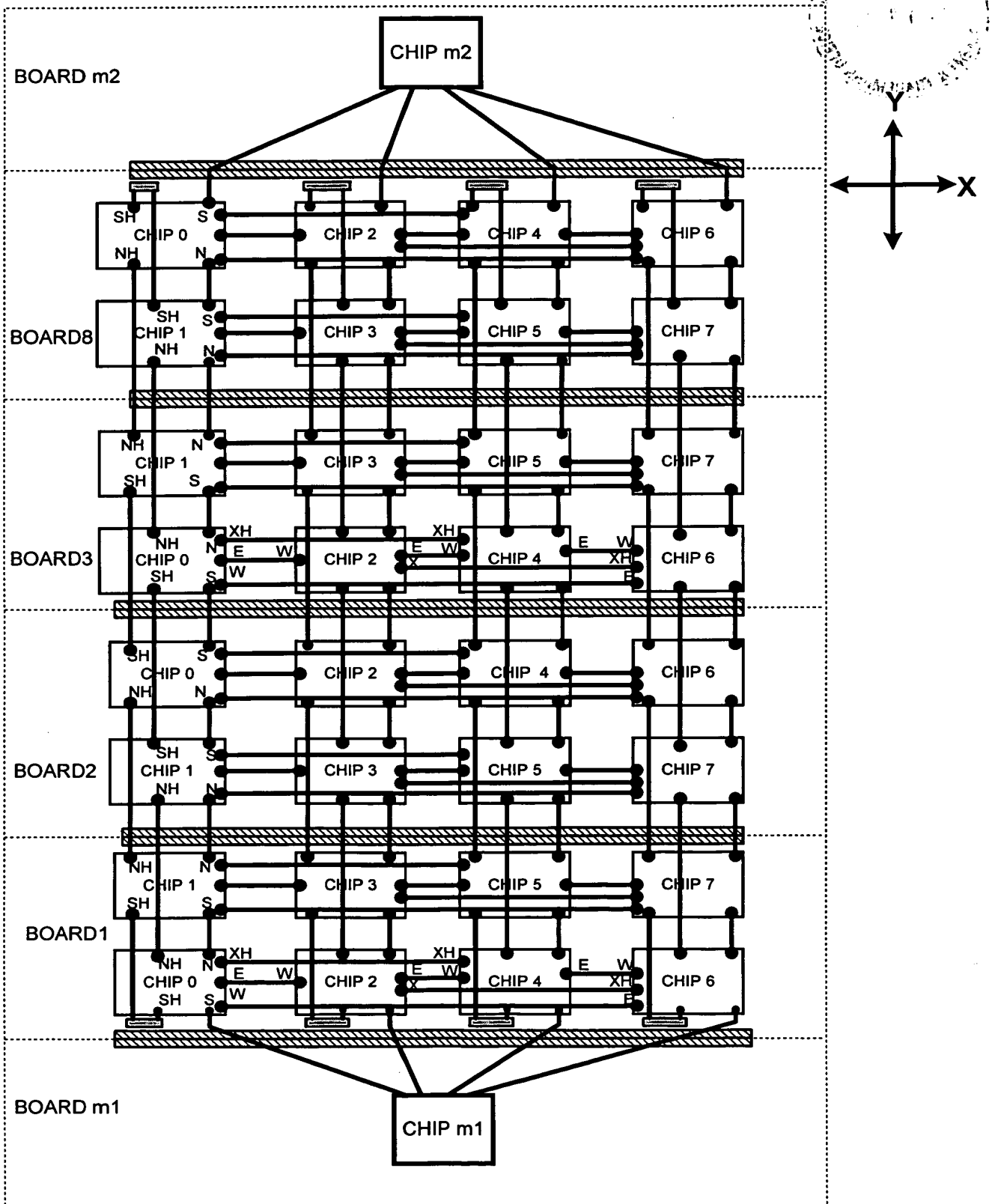


FIG. 74

SHIFT REGISTER

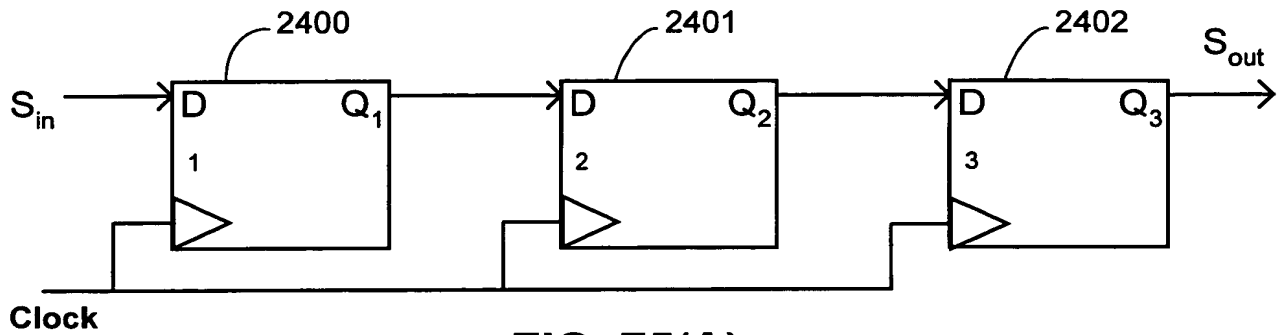


FIG. 75(A)

HOLD TIME ASSUMPTION FOR SHIFT REGISTER

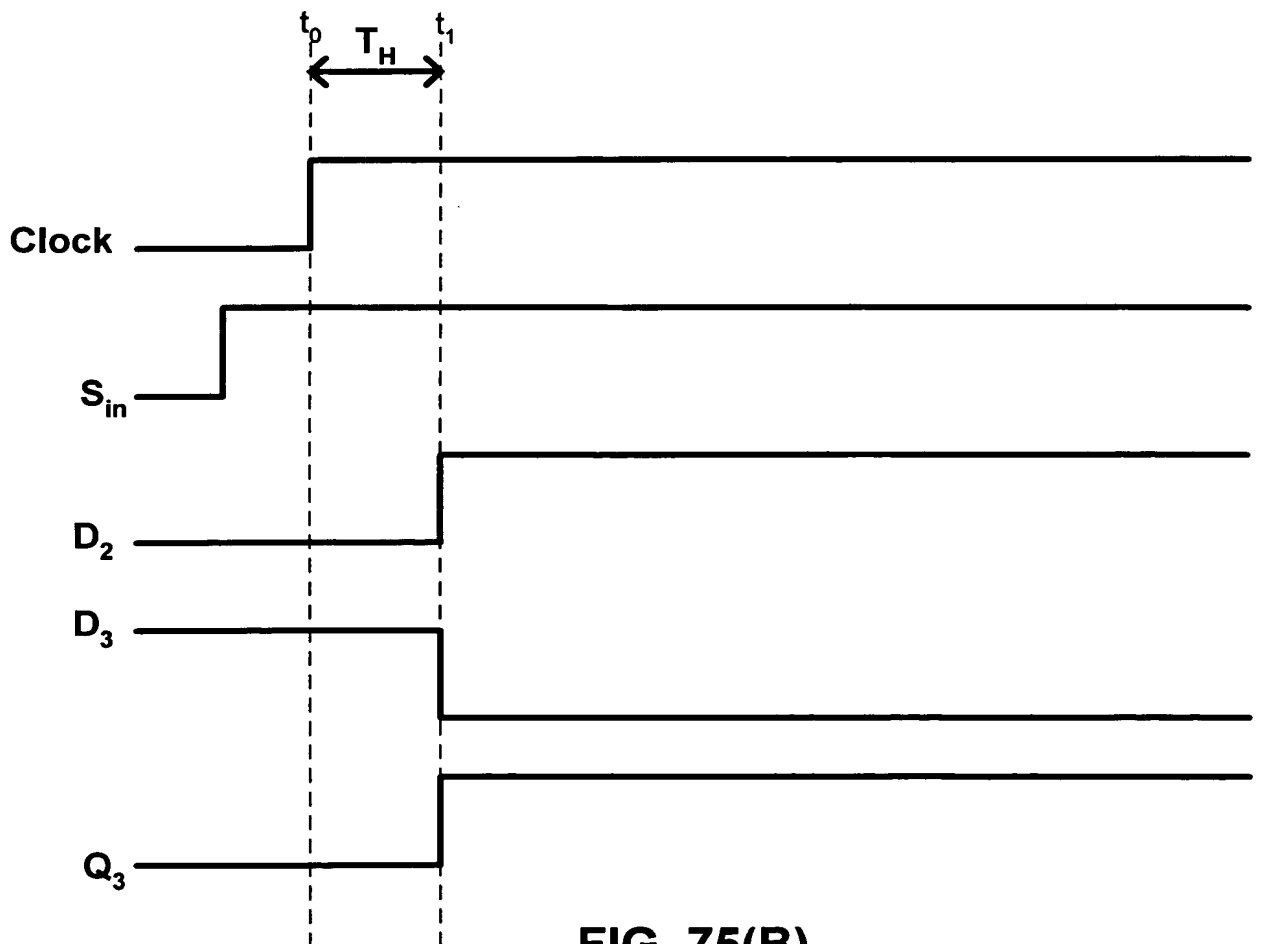
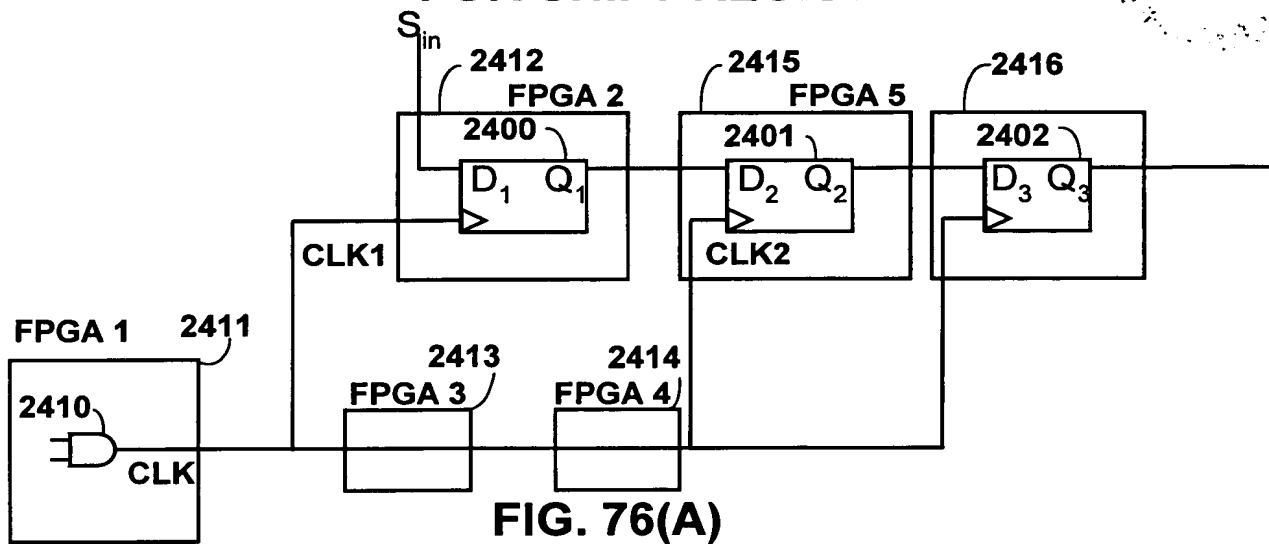
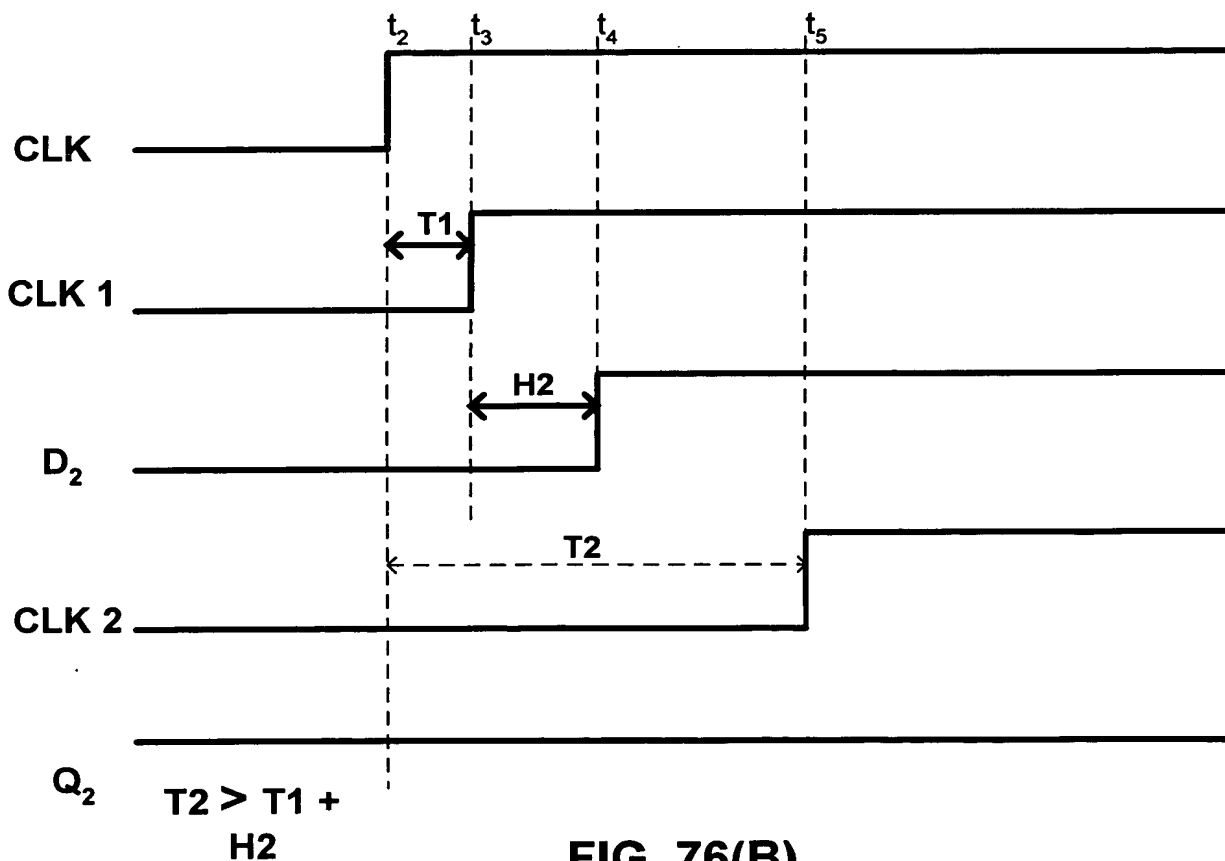


FIG. 75(B)

MULTIPLE FPGA MAPPING FOR SHIFT REGISTER



HOLD TIME VIOLATION BY LONG CLOCK SKEW



CLOCK GLITCH PROBLEM

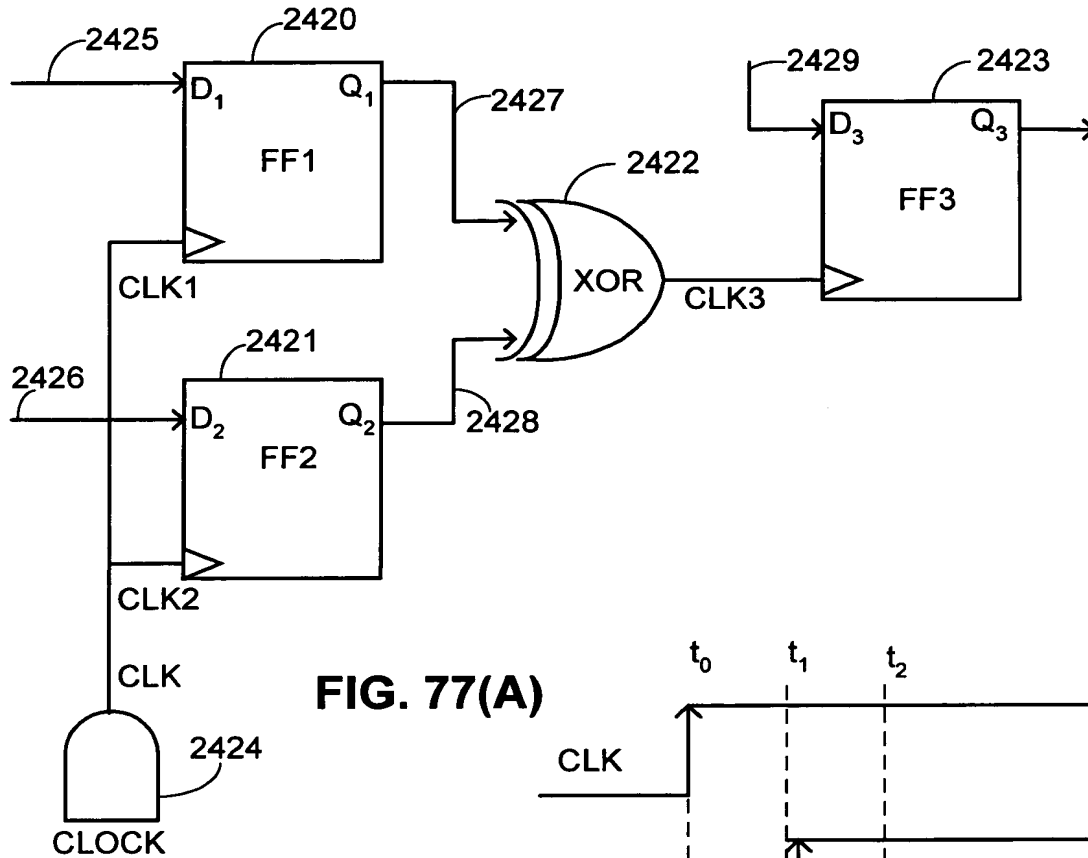


FIG. 77(A)

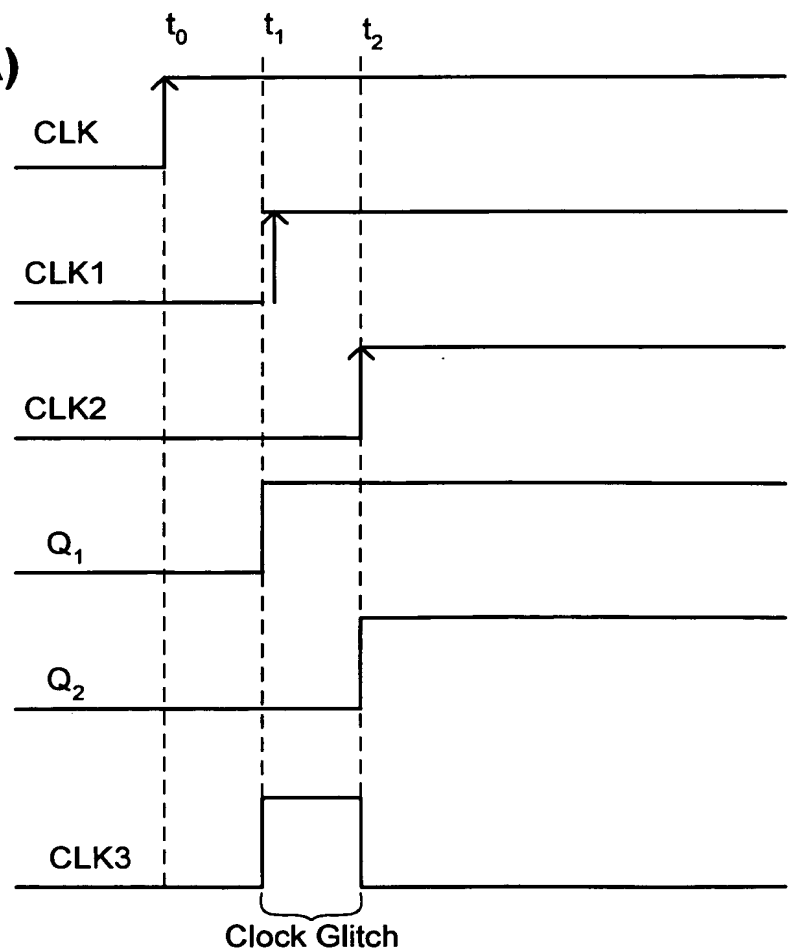
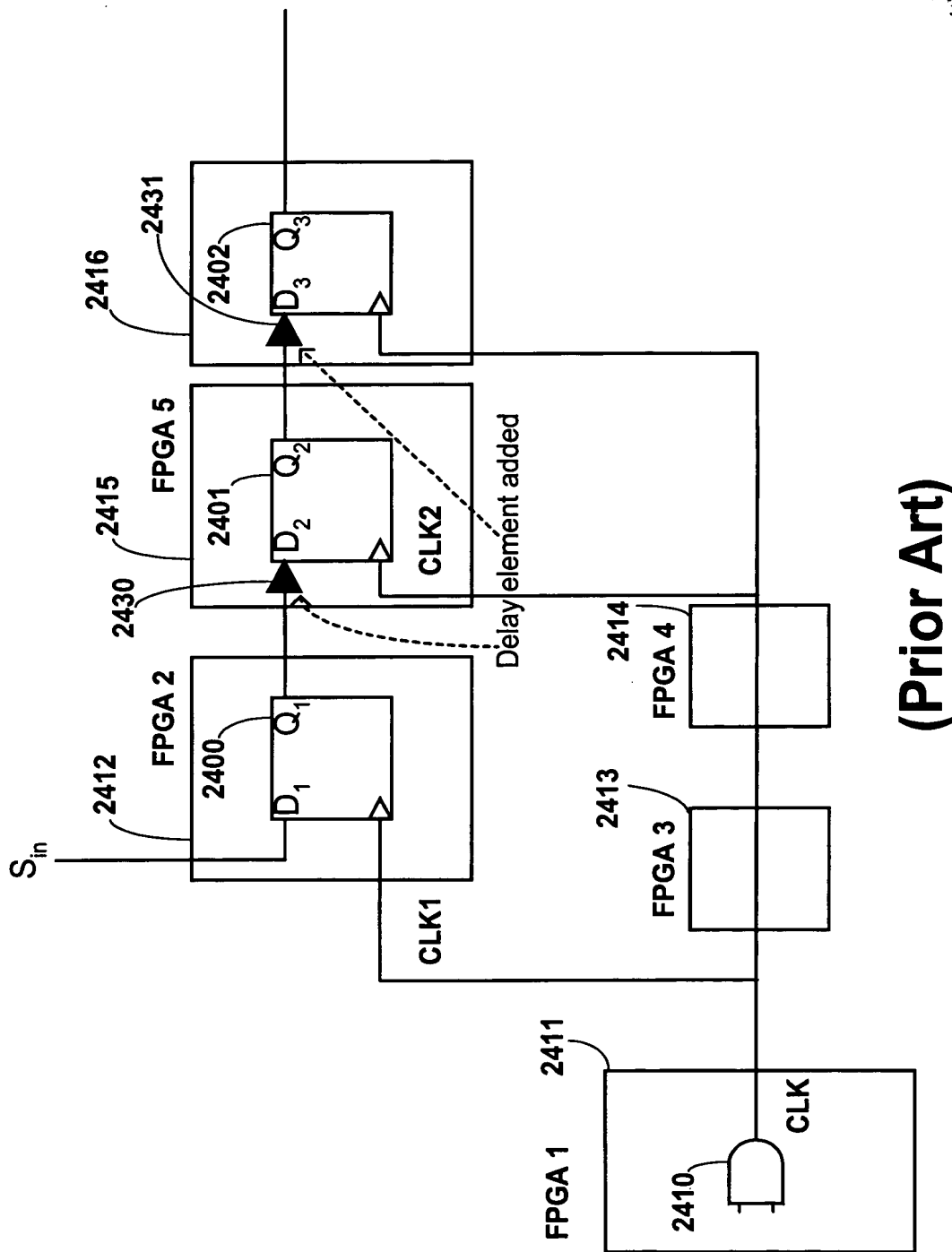


FIG. 77(B)

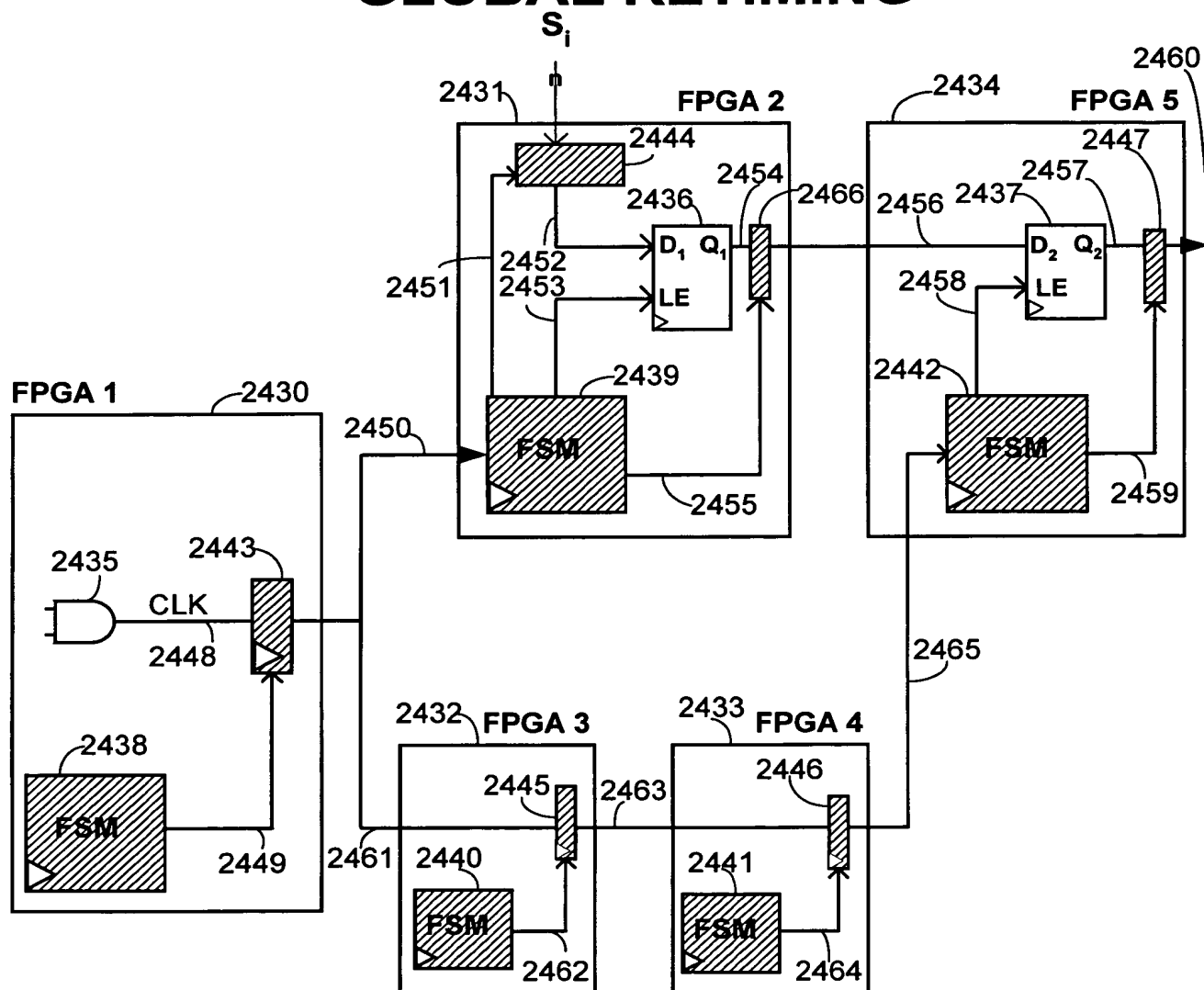
TIMING ADJUSTMENT BY ADDING DELAY



(Prior Art)

FIG. 78

GLOBAL RETIMING



Legend

△ Controlled by the global reference clock.

▨ FSM and I/O registers for retiming control.

(Prior Art)

FIG. 79

TIGF LATCH

Original Latch

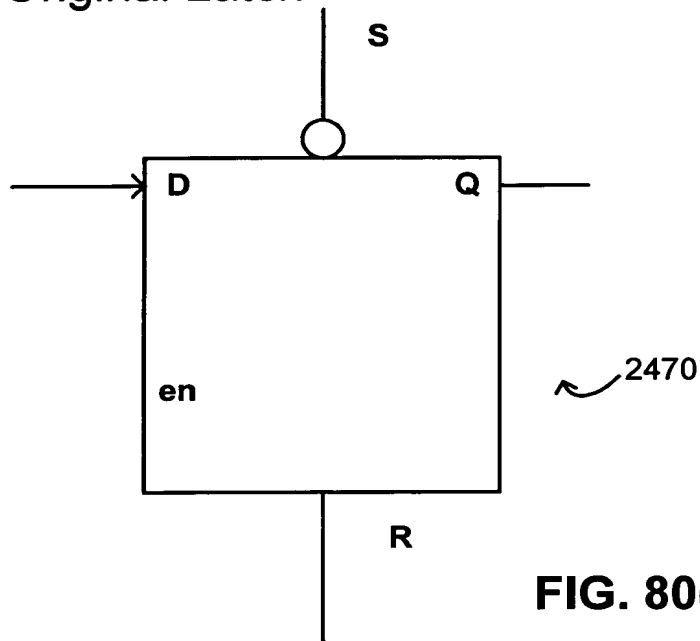


FIG. 80(A)

TIGF Latch

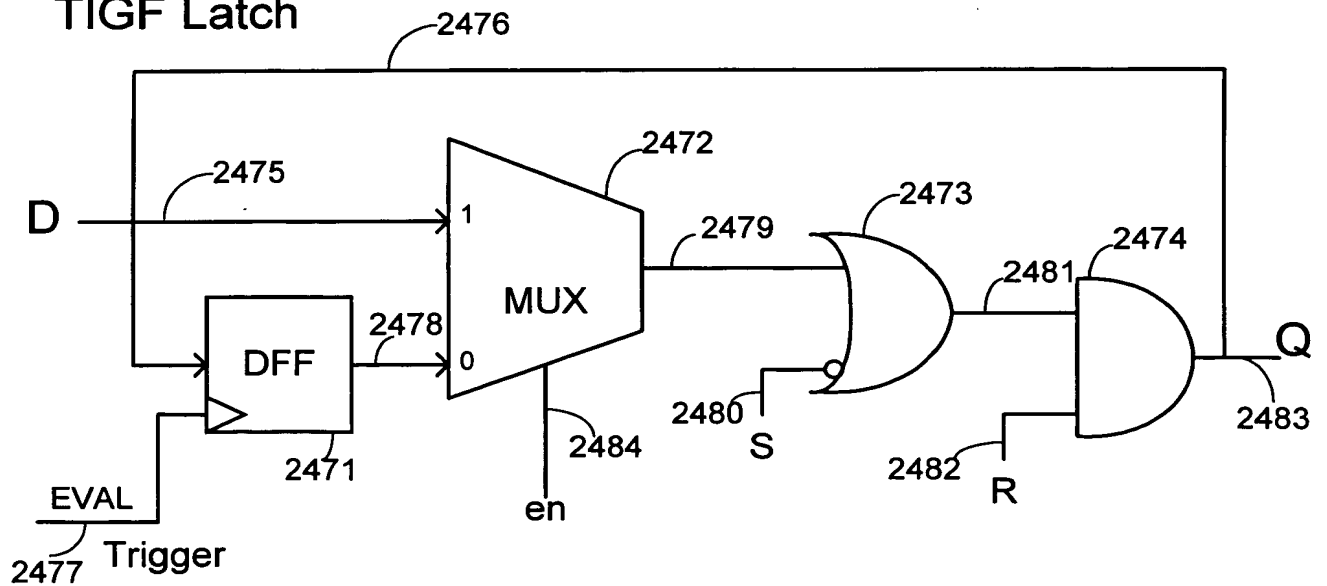
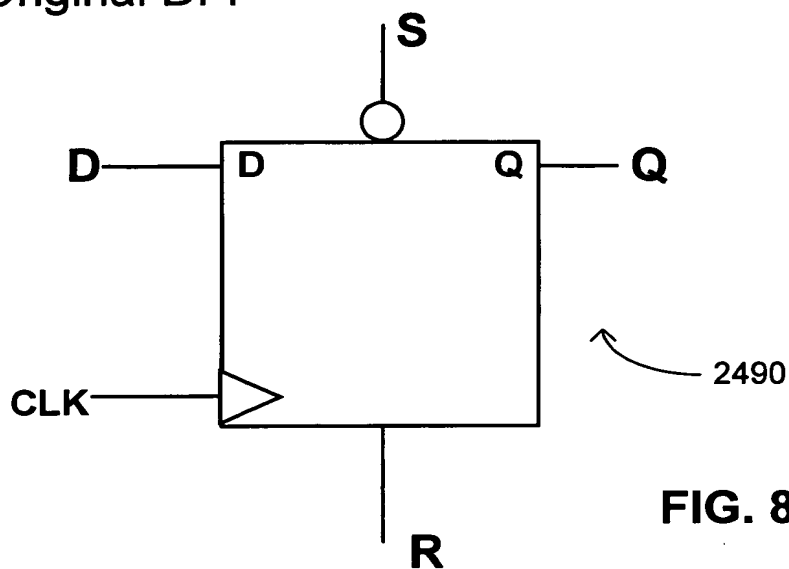


FIG. 80(B)

Original DFF



TIGF DFF

FIG. 81(A)

TIGF DFF and Edge Detector

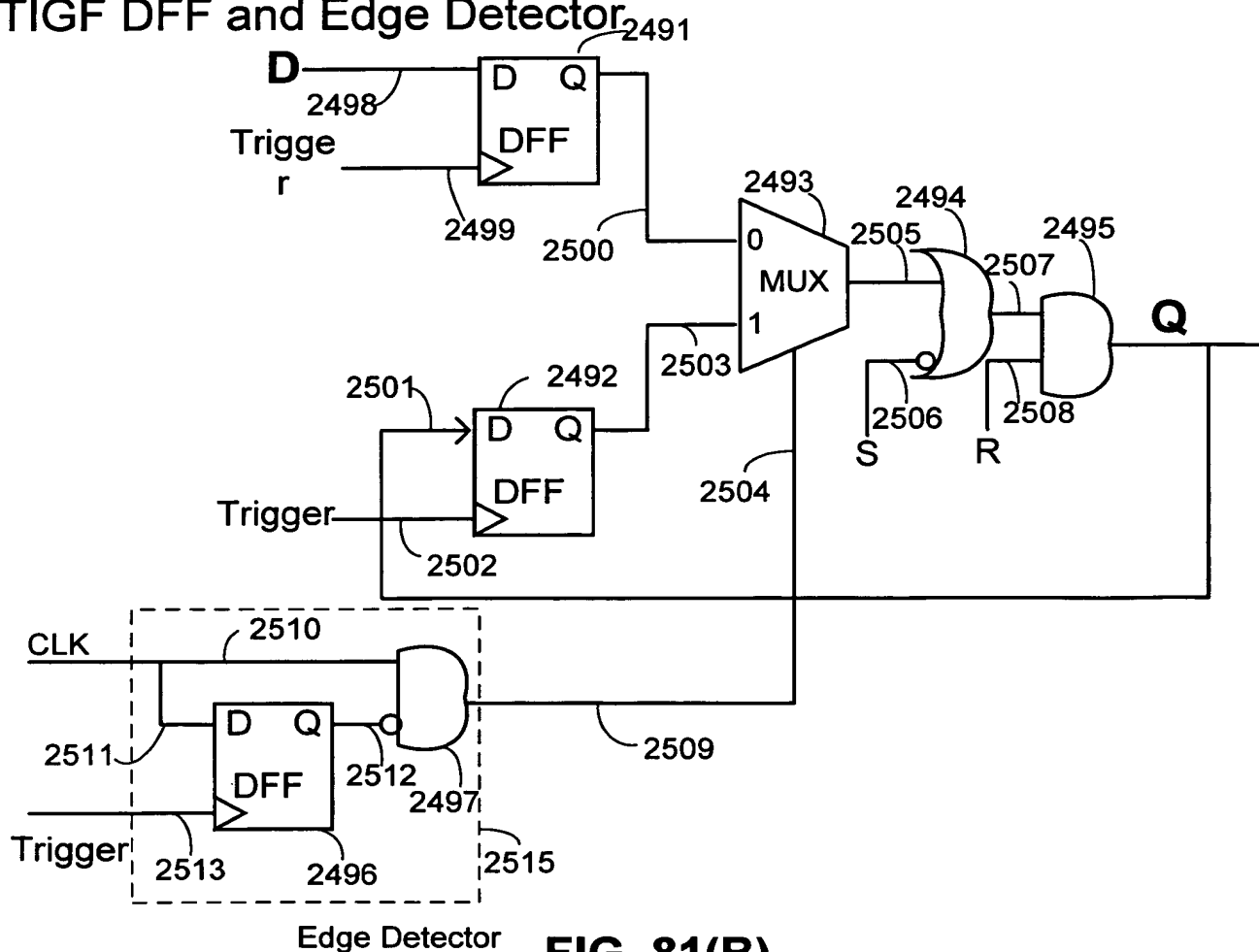


FIG. 81(B)

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GLOBAL TRIGGER SIGNAL

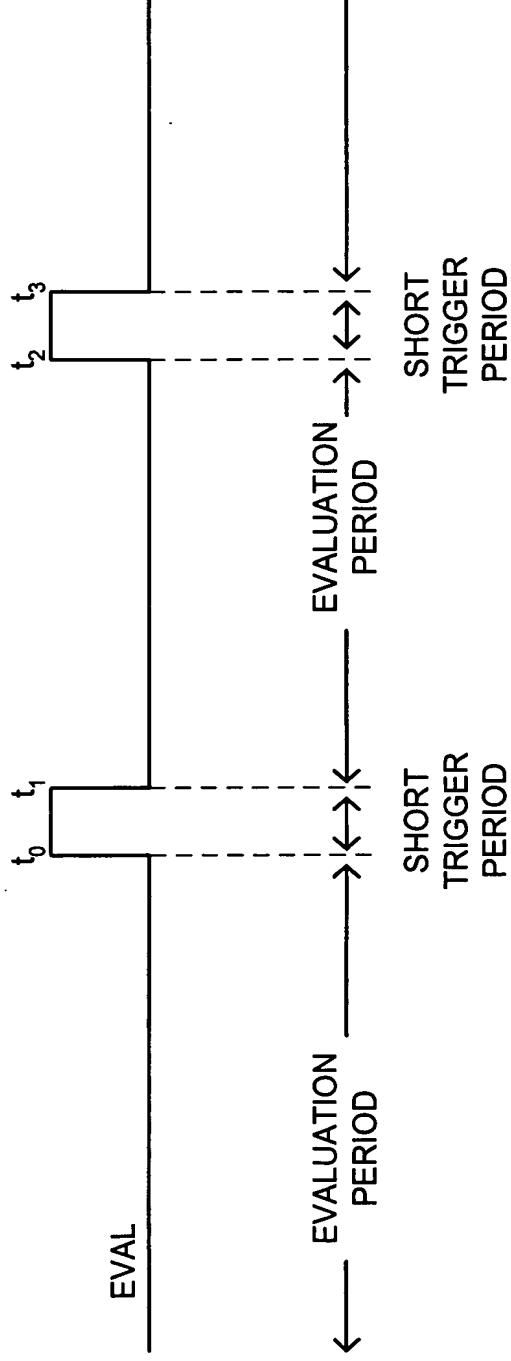


FIG. 82



RCC System

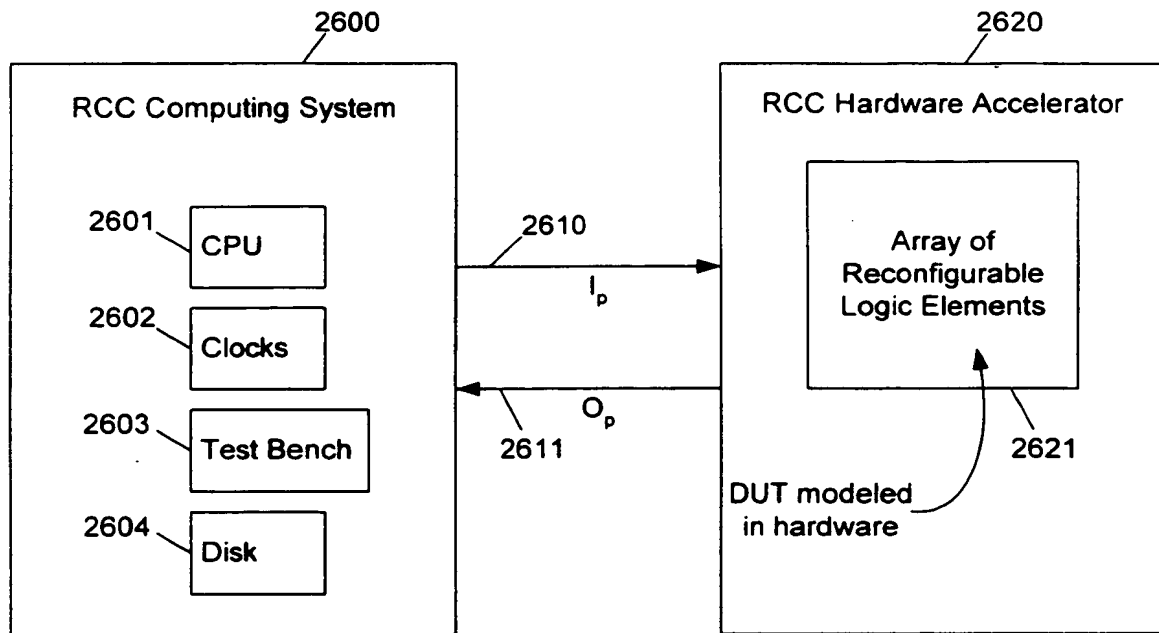


FIG. 83

0900124-101001

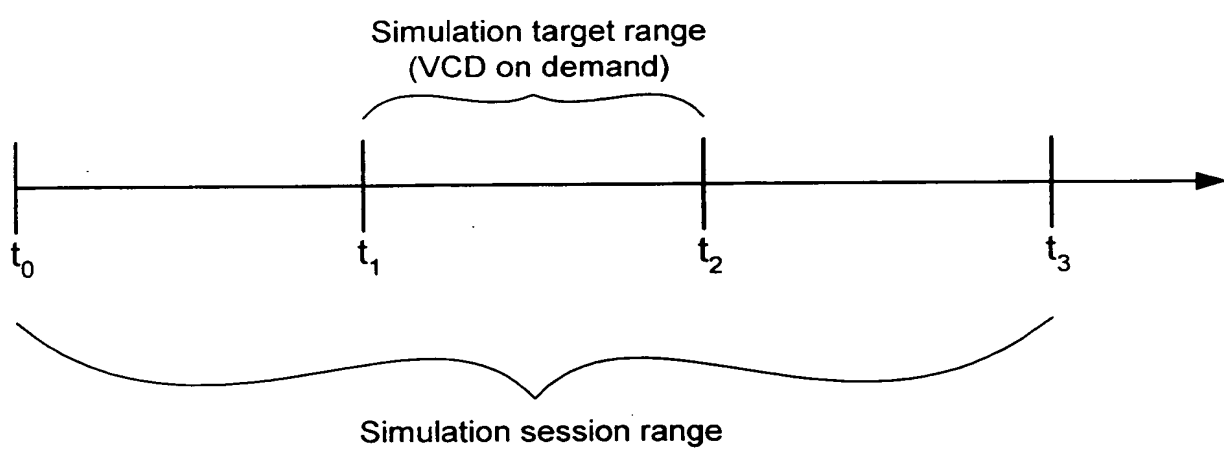


FIG. 84

SINGLE-ROW FPGA PER BOARD

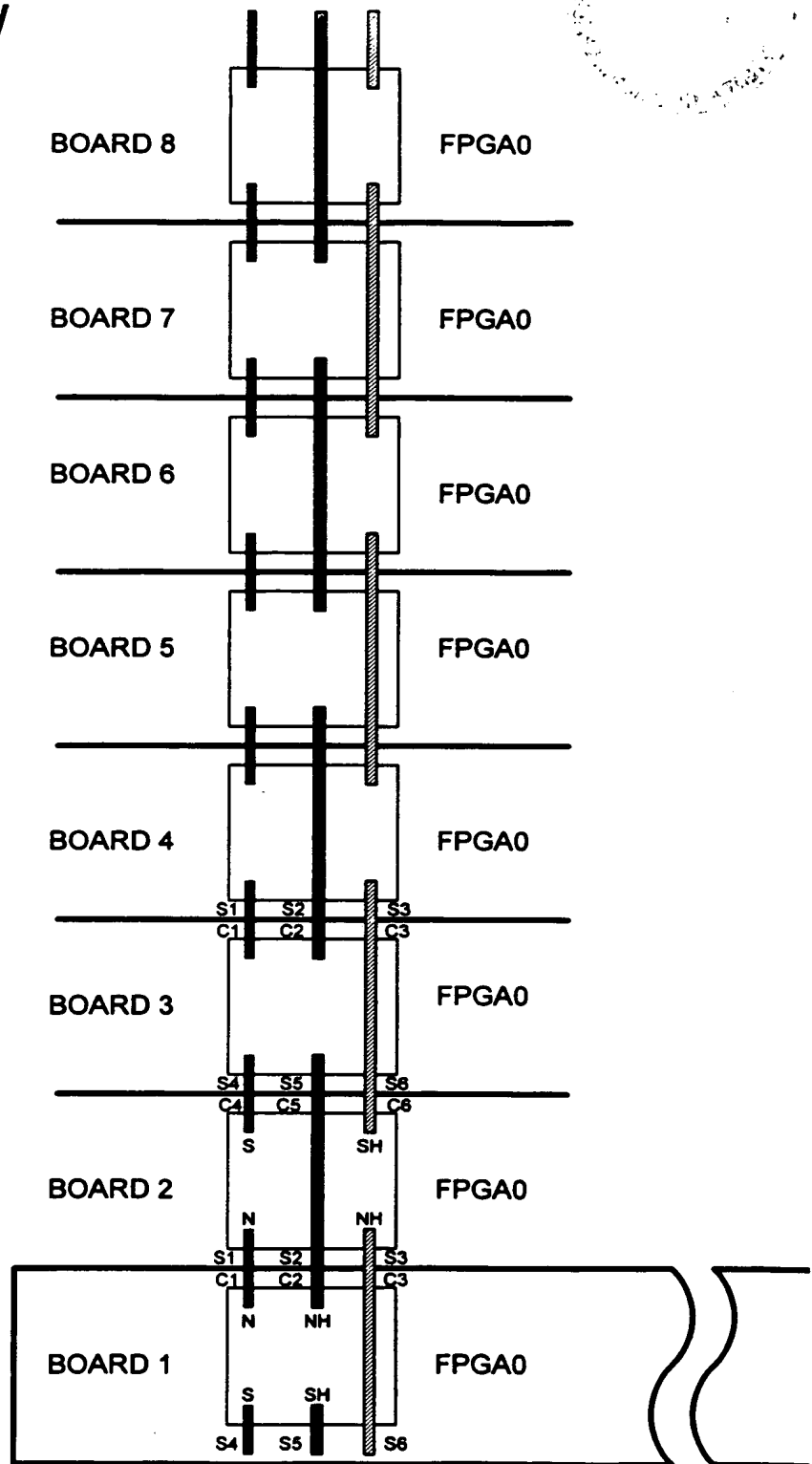


FIG. 85

TWO-ROW FPGA PER BOARD

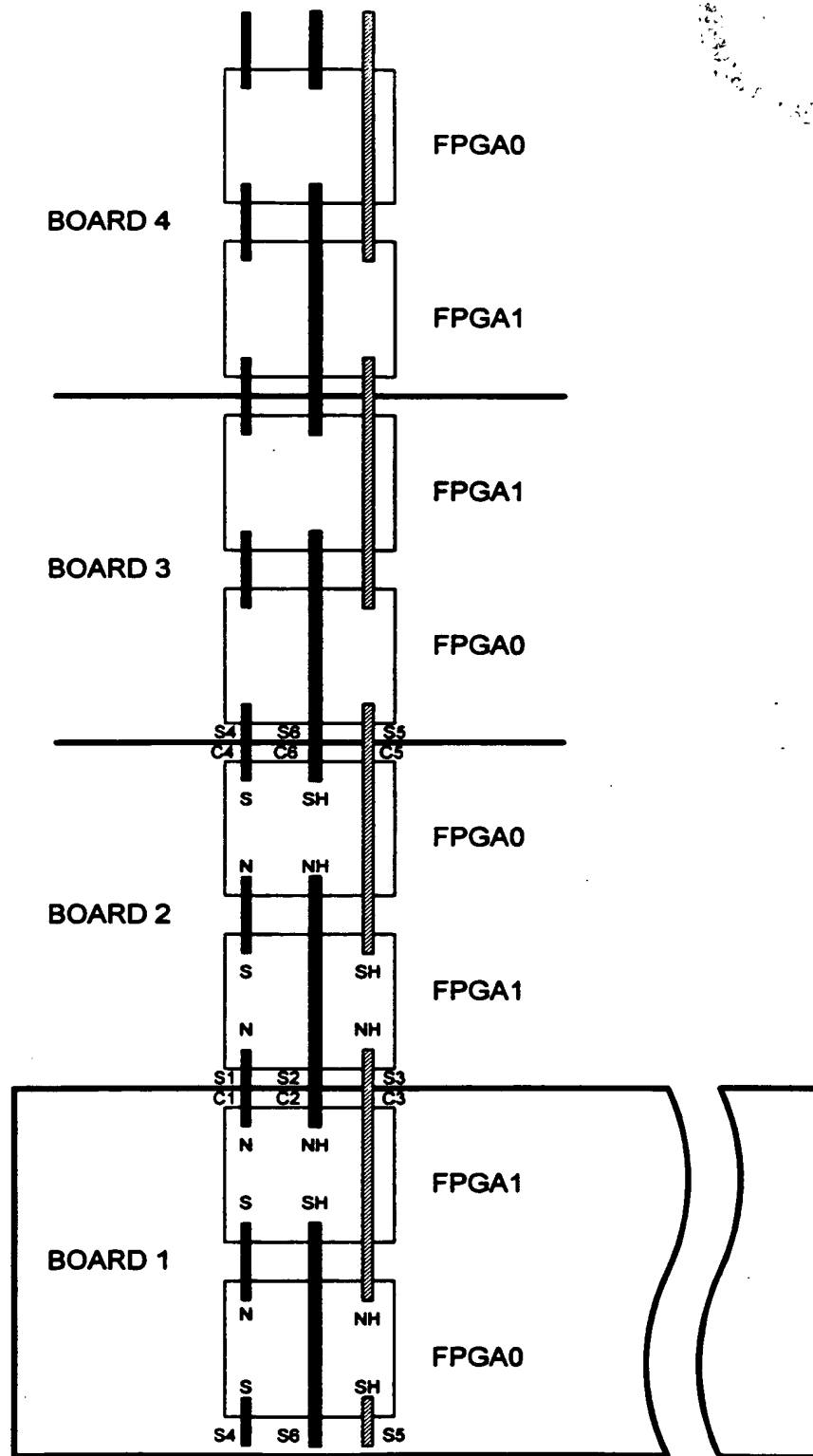


FIG. 86

THREE-ROW FPGA PER BOARD

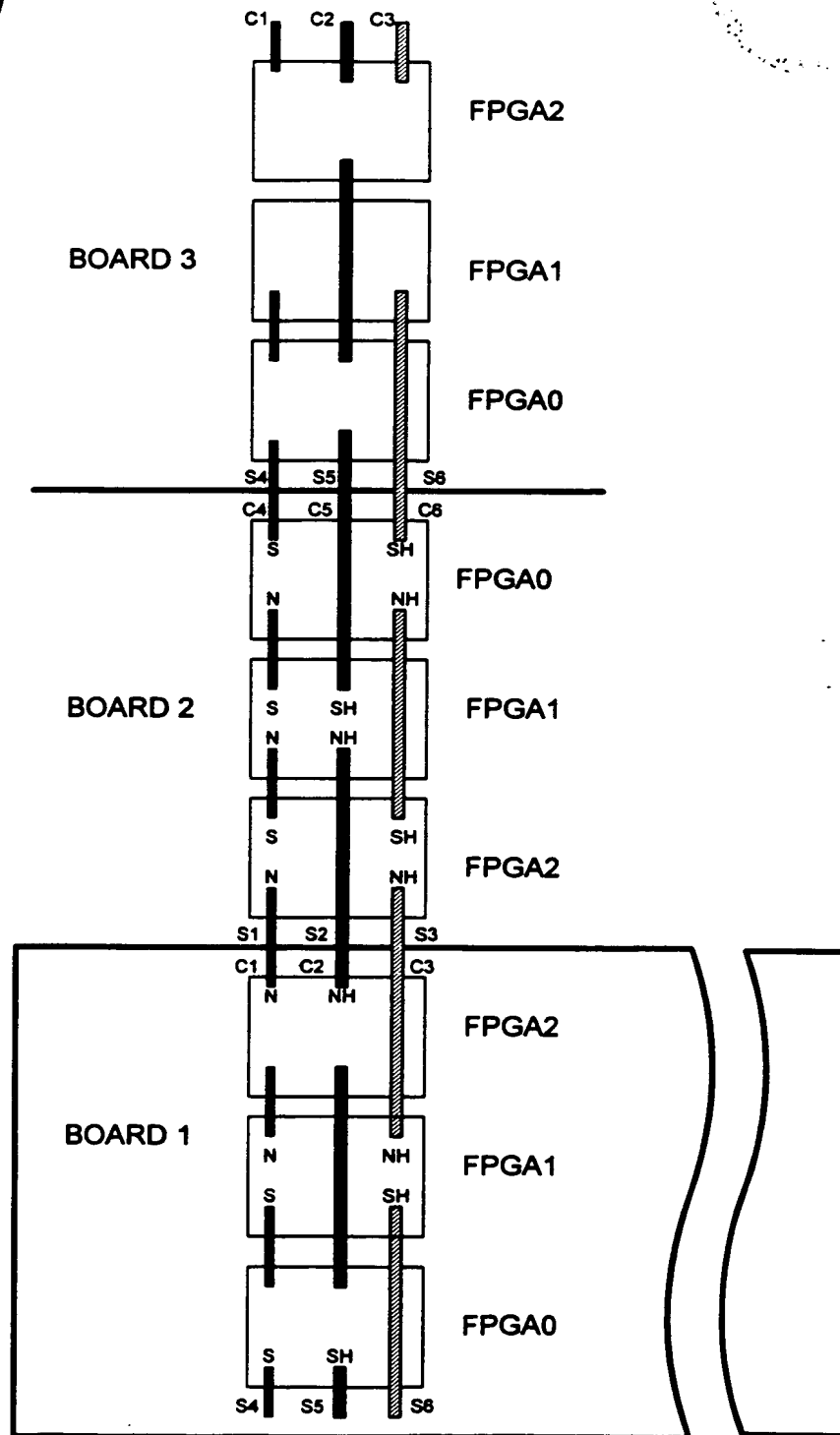


FIG. 87

09900124 101001

FOUR-ROW FPGA PER BOARD

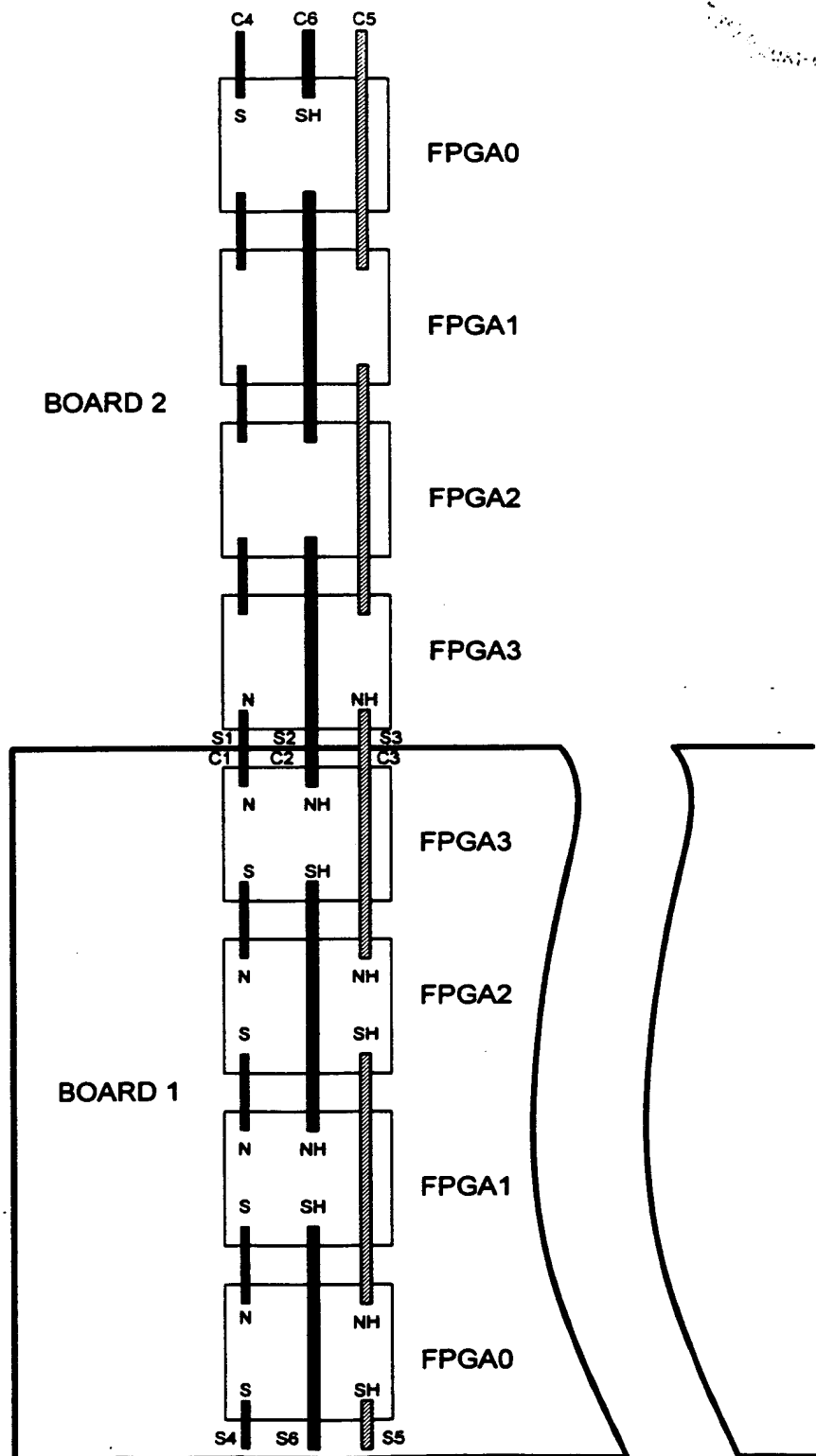


FIG. 88

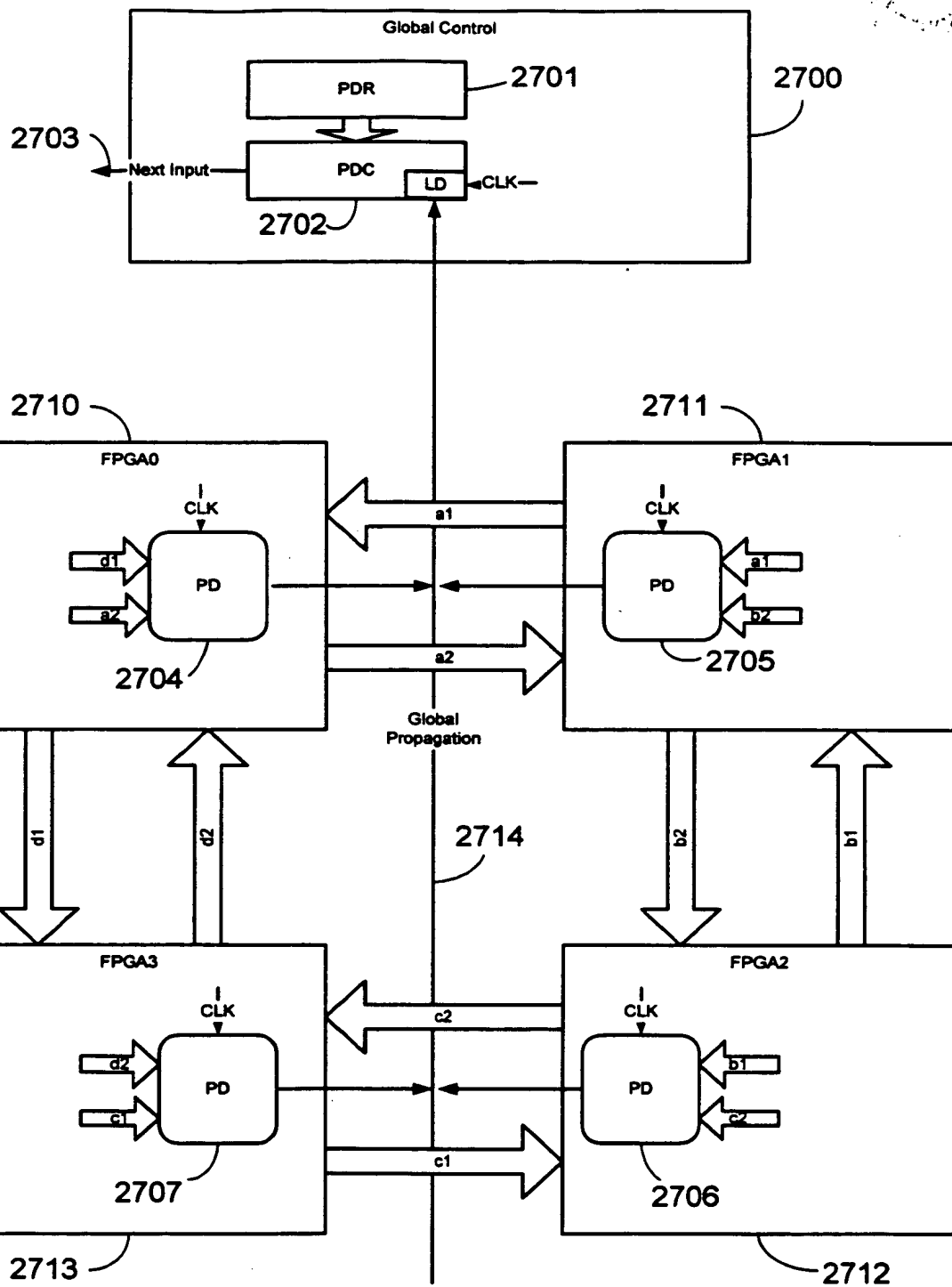


FIG. 90

09900124-101001

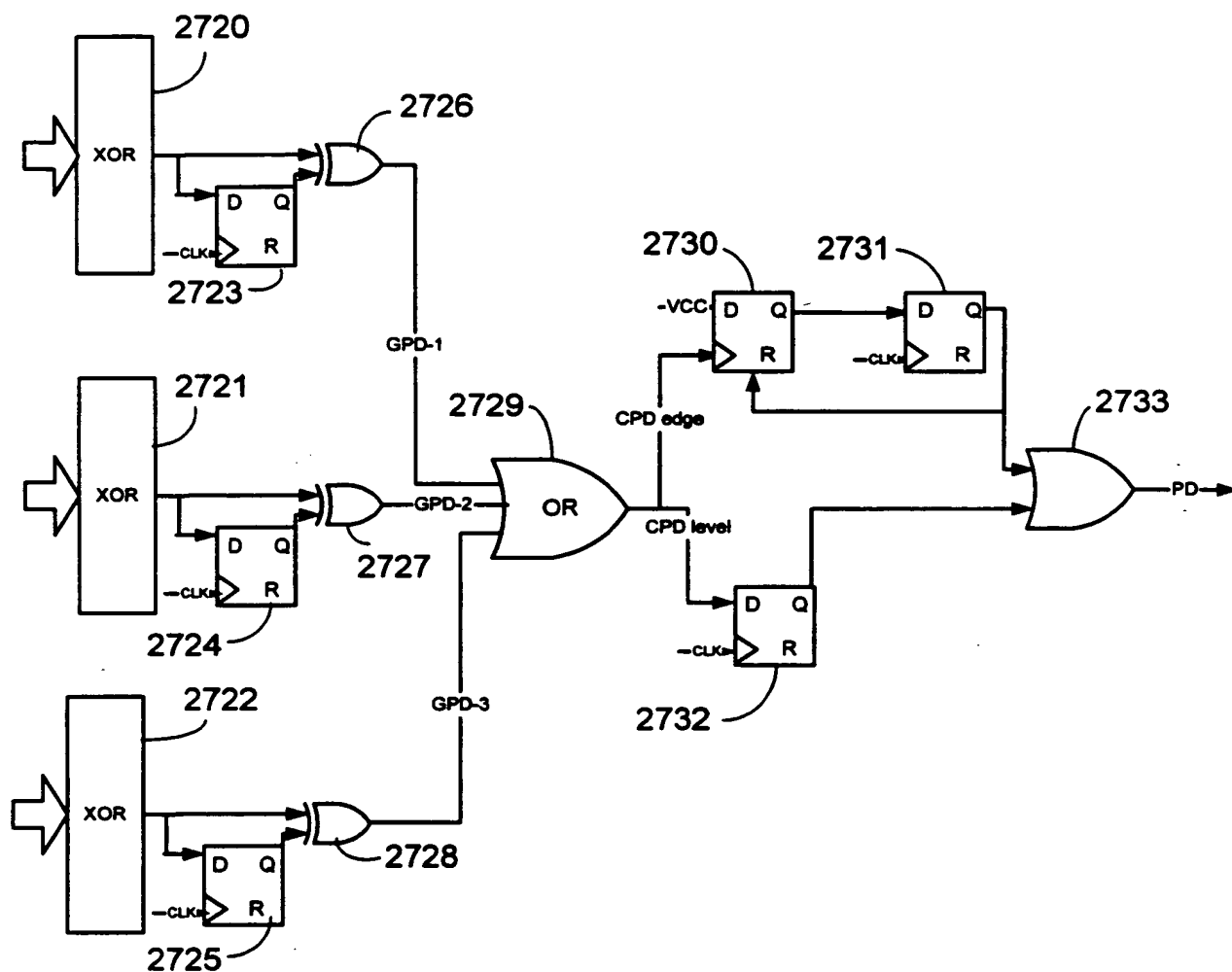


FIG. 91

0900124-101001

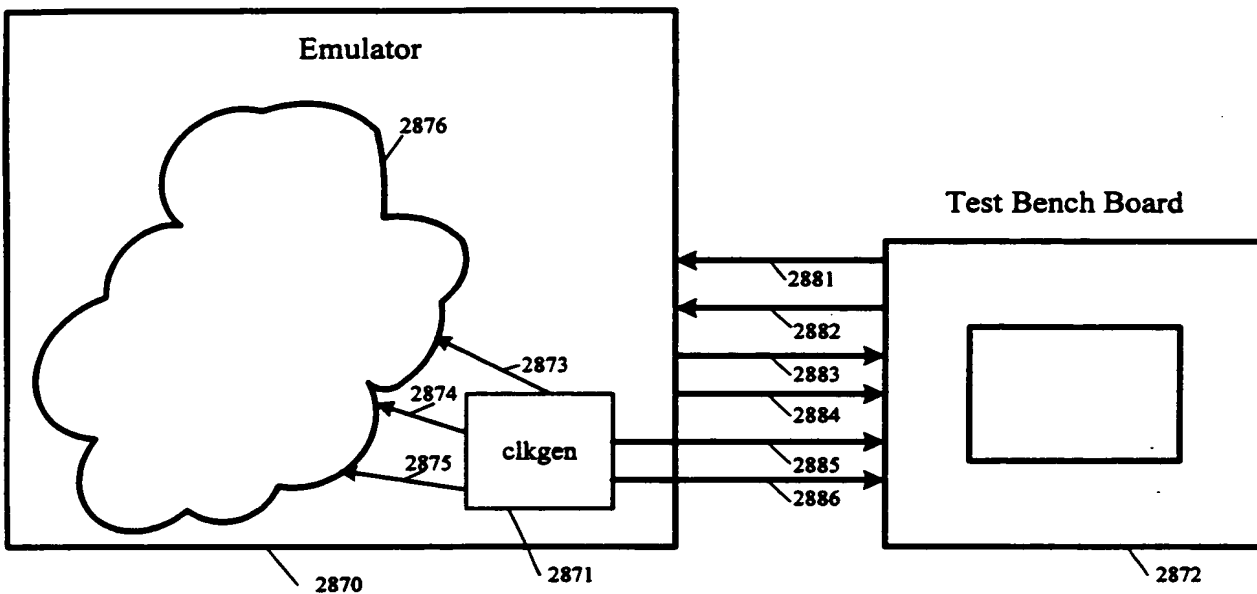


FIG. 92

Clock Specification

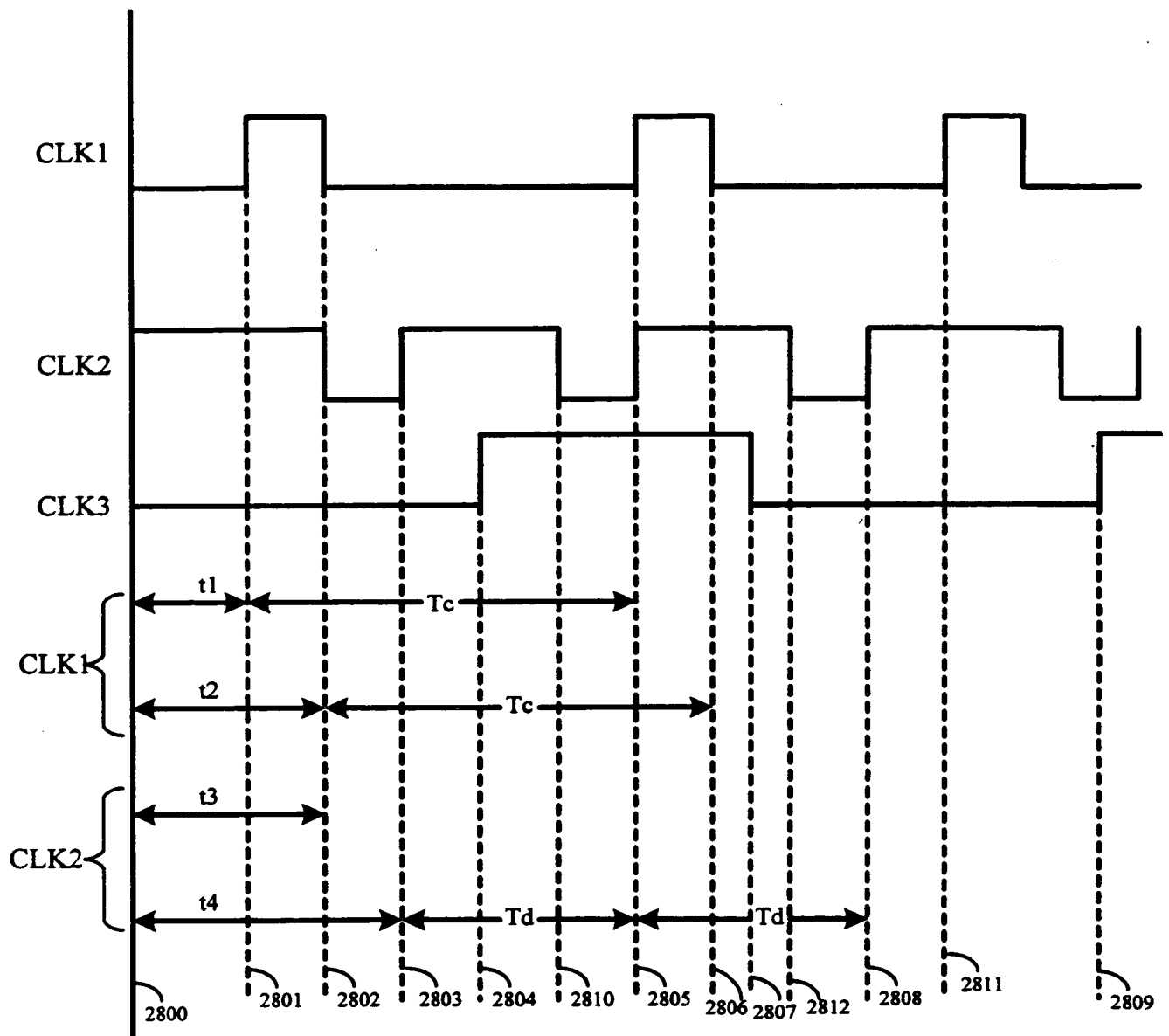


FIG. 93

Clock Generation Scheduler w/ Slices

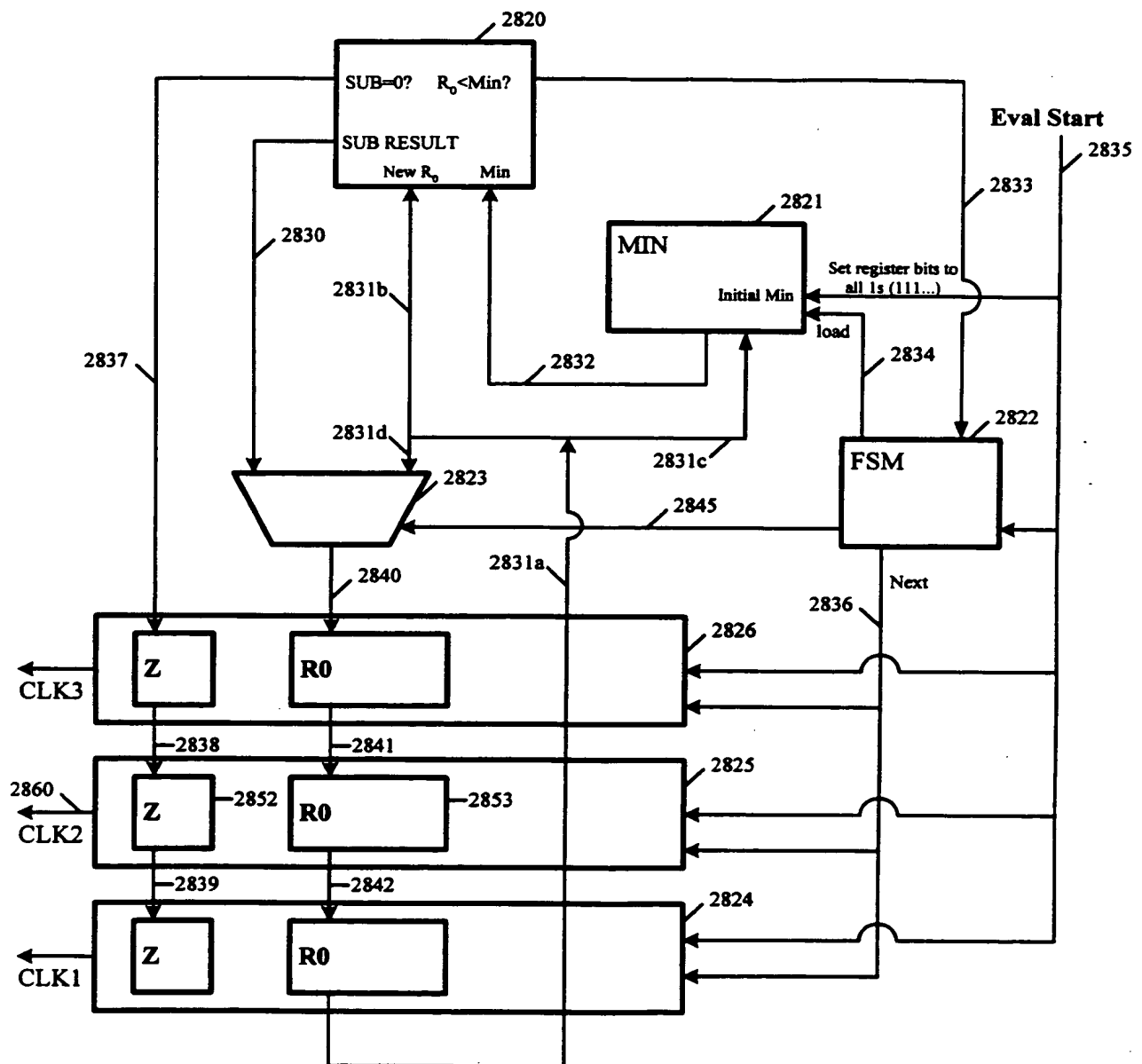


FIG. 94

Clock Generation Slice

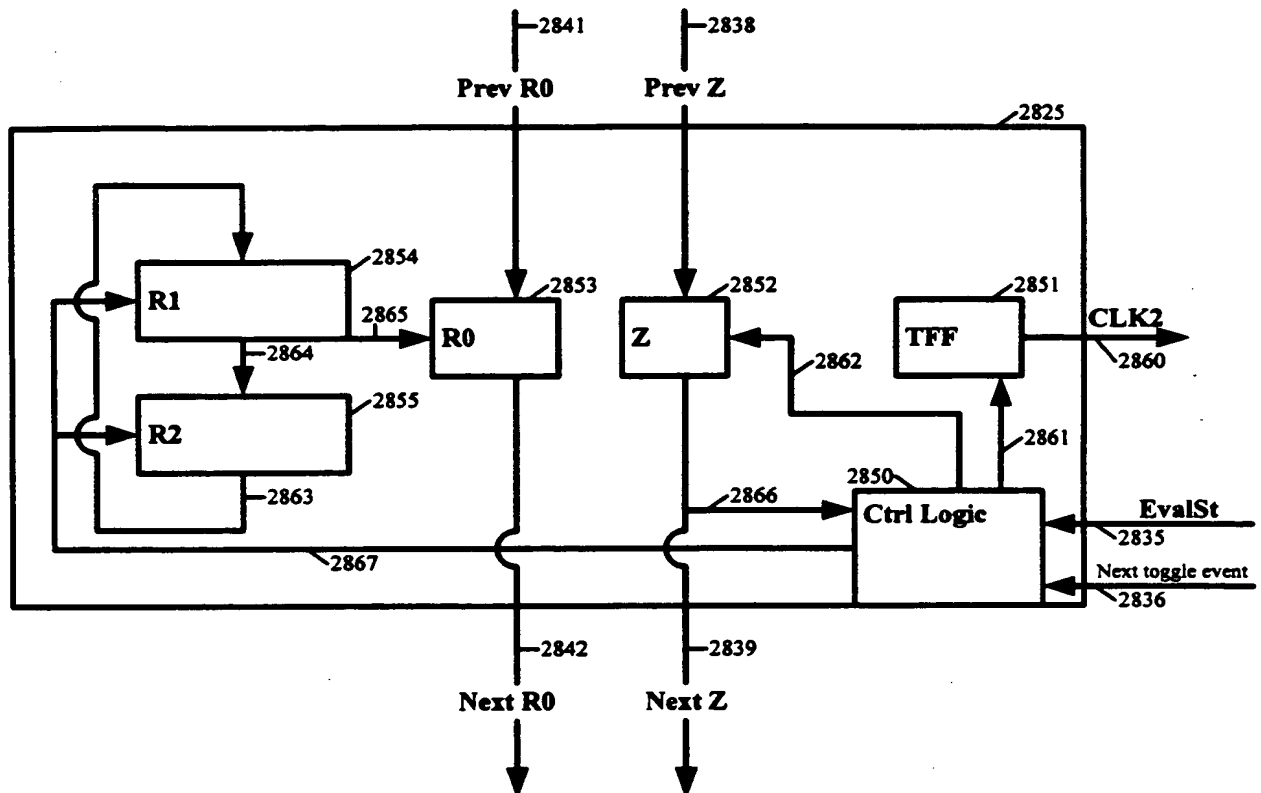


FIG. 95

Clock Generation Scheduler and Slices

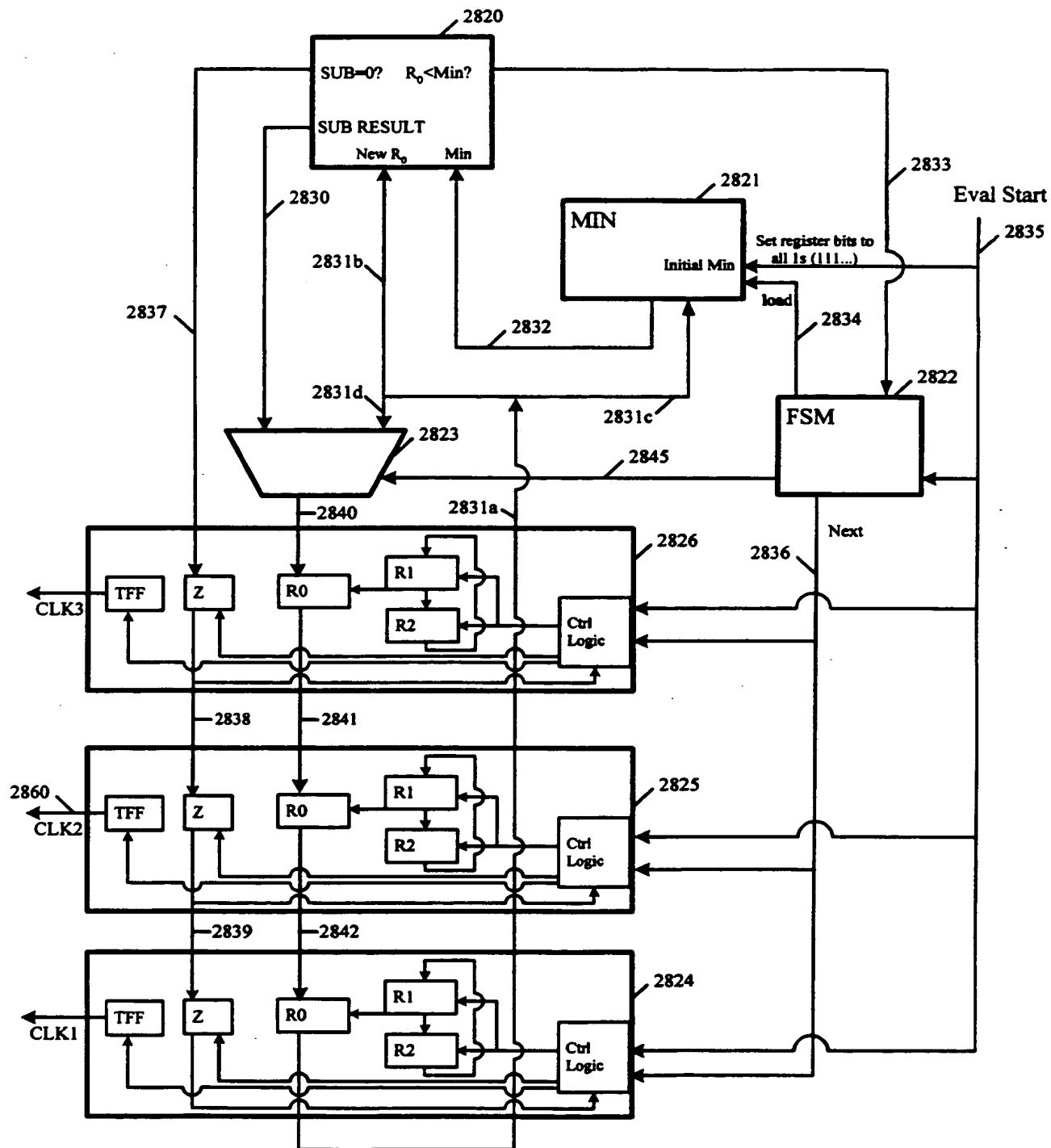


FIG. 96

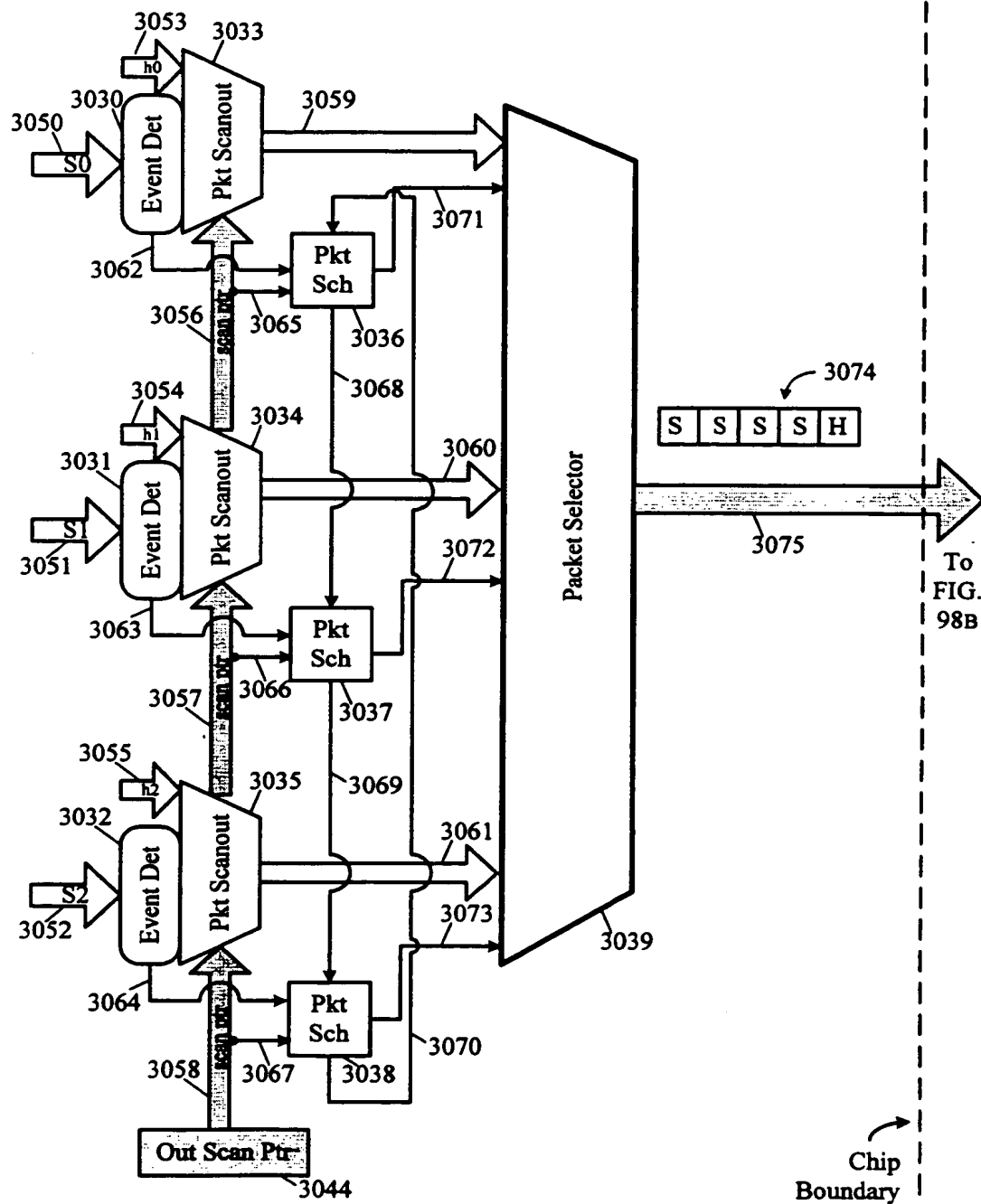


FIG. 98A

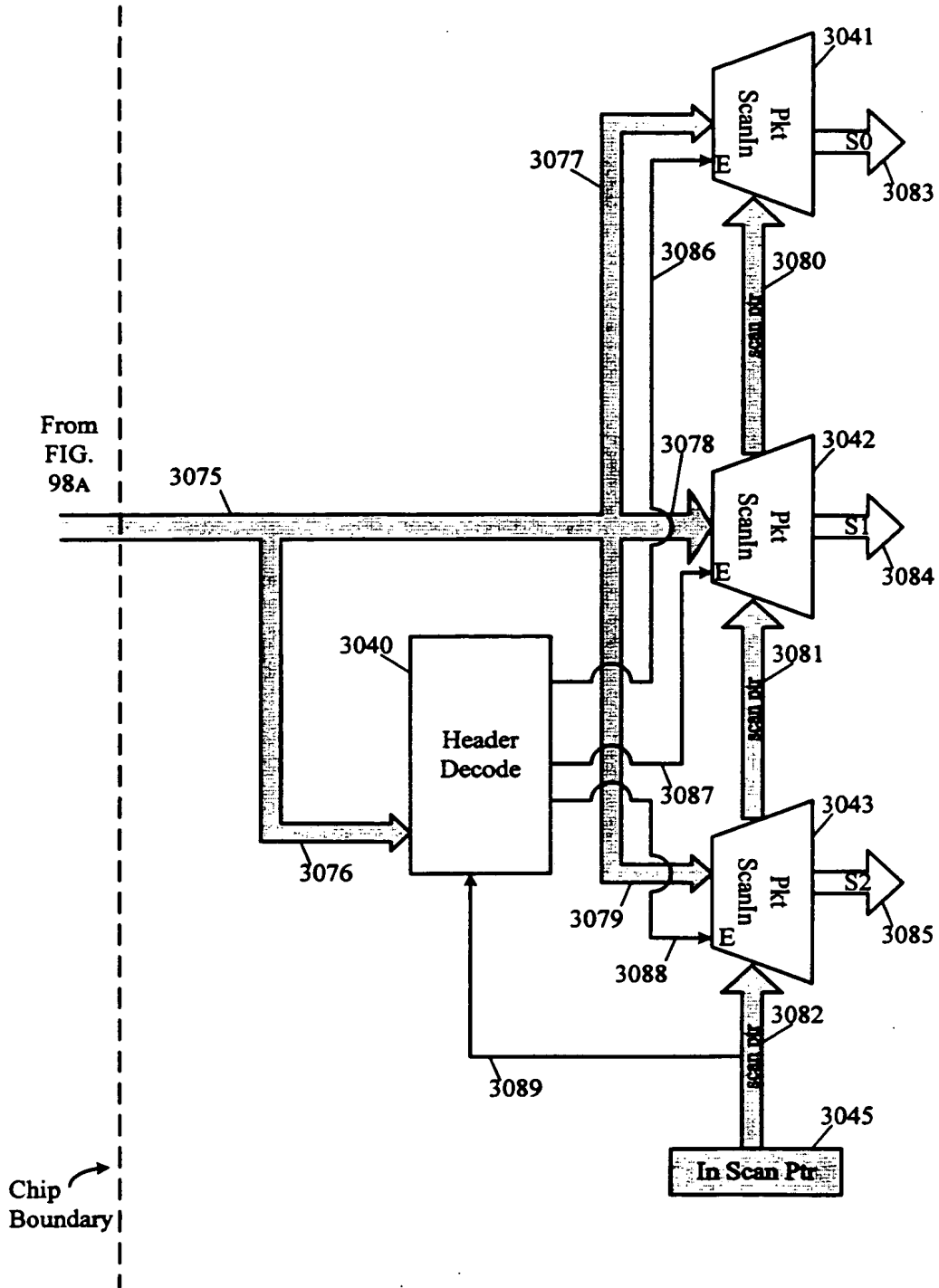


FIG. 98B